Service Manual

Tektronix

CTS 850 Test Set
SDH/PDH, Jitter & Wander

070-9991-00

Note: This manual is only valid for those units containing a software version of V2.8 and above.

Warning

The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to the Safety Summary prior to performing service.

Tektronix, Inc., P.O. Box 1000, Wilsonville, OR 97070-1000

WARRANTY

Tektronix warrants that this product will be free from defects in materials and workmanship for a period of three (3) years from the date of shipment. If any such product proves defective during this warranty period, Tektronix, at its option, either will repair the defective product without charge for parts and labor, or will provide a replacement in exchange for the defective product.

In order to obtain service under this warranty, Customer must notify Tektronix of the defect before the expiration of the warranty period and make suitable arrangements for the performance of service. Customer shall be responsible for packaging and shipping the defective product to the service center designated by Tektronix, with shipping charges prepaid. Tektronix shall pay for the return of the product to Customer if the shipment is to a location within the country in which Tektronix service center is located. Customer shall be responsible for paying all shipping charges, duties, taxes, and any other charges for products returned to any other locations.

This warranty shall not apply to any defect, failure or damage caused by improper use or improper or inadequate maintenance and care. Tektronix shall not be obligated to furnish service under warranty a) to repair damage resulting from attempts by personnel other than Tektronix representatives to install, repair or service the product; b) to repair damage resulting from improper user or connection to incompatible equipment; or c) to service a product that has been modified or integrated with other products when the effect of such modification or integration increases the time or difficulty of servicing the product.

THIS WARRANTY IS GIVEN BY TEKTRONIX WITH RESPECT TO THIS PRODUCT IN LIEU OF ANY OTHER WARRANTIES, EXPRESSED OR IMPLIED. TEKTRONIX AND ITS VENDORS DISCLAIM ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. TEKTRONIX' RESPONSIBILITY TO REPAIR OR REPLACE DEFECTIVE PRODUCTS IS THE SOLE AND EXCLUSIVE REMEDY PROVIDED TO THE CUSTOMER FOR BREACH OF THIS WARRANTY. TEKTRONIX AND ITS VENDORS WILL NOT BE LIABLE FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES IRRESPECTIVE OF WHETHER TEKTRONIX OR THE VENDOR HAS ADVANCE NOTICE OF THE POSSIBILITY OF SUCH DAMAGES.

How to Reach Customer Service

Tektronix provides high quality Technical Support on applications, operation, measurement specifications, hardware, and software by expert application engineers. If you have any questions regarding the operation, maintenance, repair, or application of your Tektronix equipment, contact your local sales and service office.

For more information on Tektronix equipment and support services, refer to the Tektronix web-site at www.tektronix.com or call 1-800-Tek-Wide.

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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any equipment connected to it. To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of the system. Read the *General Safety Summary* in other system manuals for warnings and cautions related to operating the system.

Injury Precautions

Use Proper Power Cord
To avoid fire hazard, use only the power cord specified for this product.

Avoid Electric Overload
To avoid electric shock or fire hazard, do not apply a voltage to a terminal that is outside the range specified for that terminal.

Ground the product
This product is grounded through the grounding conductor of the power cord. To avoid electric shock, the grounding conductor must be connected to earth ground. Before making connections to the input or output terminals of the product, ensure that the product is properly grounded.

Do not operate without covers
To avoid electric shock or fire hazard, do not operate this product with covers or panels removed.

Use Proper Fuse
To avoid fire hazard, use only the fuse type and rating specified for this product.

Do not operate in Wet/Damp Conditions
To avoid electric shock, do not operate this product in wet or damp conditions.

Do not operate in Explosive Atmosphere
To avoid injury or fire hazard, do not operate this product in an explosive atmosphere.

Wear Eye Protection
To avoid eye injury, wear eye protections if there is a possibility of exposure to high-intensity rays.

Product Damage Precautions

Use Proper Power Source

Do not operate this product from a power source that applies more than the voltage specified.

Provide Proper Ventilation

To prevent product overheating, provide proper ventilation.

Do not operate with suspected failures

If you suspect there is damage to this product, have it inspected by qualified service personnel.

Safety Terms and Symbols

Terms in this manual

These terms may appear in this manual:

WARNING: *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION: *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Terms on the Product

These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product

The following symbols may appear on the product:

DANGER - High Voltage

Protective Ground (Earth) Terminal

ATTENTION - Refer to Manual

Double Insulated

Certifications and Compliances

CSA Certified Power Cords

CSA Certification includes the products and power cords appropriate for use in the North American power network. All other power cords supplied are approved for the country of use.

Service Safety Summary

Only qualified personnel should perform service procedures. Read this *Service Safety Summary* and the *General Safety Summary* before performing any service procedures.

Do Not Service Alone

Do not perform internal service or adjustments of this produce unless another person capable of rendering first aid and resuscitation is present.

Disconnect Power

To avoid electric shock, disconnect the main power by means of the power cord of, if provided, the power switch.

Use Caution When Servicing the CRT

To avoid electric shock or injury, use extreme caution when handling the CRT. Only qualified personnel familiar with CRT servicing procedures and precautions should remove or install the CRT.

CRTs retain hazardous voltages for long periods of time after power is turned off. Before attempting any servicing, discharge the CRT by shorting the anode to chassis ground. When discharging the CRT, connect the discharge path to ground and then the anode. Rough handling may cause the CRT to implode. Do not nick or scratch the glass or subject it to undue pressure when removing or installing it. When handling the CRT, wear safety goggles and heavy gloves for protection.

Use Care when servicing with Power On

Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

X-Radiation

To avoid x-radiation exposure, do not modify or otherwise alter the high-voltage circuitry or the CRT enclosure. X-ray emissions generated within this product have been sufficiently shielded.

Preface

This manual explains how to verify, service, troubleshoot, and repair the CTS 850 Test Set to the module level. This manual contains the following information:

How This Manual is Organized

This manual is divided into eleven sections:

- *Specifications* lists the instrument specifications.
- *Operating Information* provides instruction on installation and gives you a brief summary of operating the CTS 850. If you need further assistance operating the test set, refer to the user manual supplied with the instrument.
- *Theory of Operation* provides general descriptions of system unit modules, sufficient to guide the technician to a faulty module.
- *Performance Verification* describes how to verify the functional performance of the test unit.
- *Adjustment Procedures* describes how to perform adjustments on the test unit.
- *Maintenance* includes procedures for the following
    - ❖ Inspection and cleaning;
    - ❖ Module removal and replacement; and,
    - ❖ General troubleshooting.
- *Options* lists the options to the test unit.
- *Electrical Parts List* provides some general information about replaceable parts for the test unit.
- *Diagrams* contains an interconnect diagram and a block diagram of CTS 850 modules.
- *Mechanical Parts List* describes the replaceable parts for the test unit
- *Glossary* lists terms used by the test unit or this manual.

Conventions

The following conventions apply throughout this manual:

- Each test procedure begins with a table, similar to the one below, that provides information you need to know before starting the test.

Equipment Required	Communications Signal Analyzer 75 Ω coaxial cable Delay line, three required
Prerequisites	All previous Physical Layer Tests
Time Required	Approximately ten minutes

- This manual presents setup instructions for the CTS in tables. Perform the steps reading from left to right in the table (see example below).

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
Begin here with Step 1	Step 2	Step 3	Step 4
		Step 5	Step 6
		Step 7	Step 8, CTS setup is complete

Menu buttons are located on the instrument front panel (see illustration on the next page). Select menu pages with the buttons below the display. Use the knob to highlight a parameter; then use the buttons at the right side to select a choice. Many setups require several iterations of highlighting parameters and selecting choices. Some setups may require more than one menu button or menu page selection as well.

Related Manuals

The following documents are available for the CTS 850 SDH/PDH Test Set:

- The CTS 850 SDH/PDH *User Manual* (Tektronix part number 070-9988-xx) is the primary source of information on how the CTS 850 functions.
- The CTS 850 SDH/PDH *Reference Manual on CD* (Tektronix part number 063-3013-xx) contains all the user manual information, in a portable electronic document format.
- The CTS 850 SDH/PDH Test Set *Programmer Manual* (Tektronix part number 070-9990-xx) describes how to control the CTS 850 using an instrument controller.
- *Wander Analyst User Manual* (Tektronix part number 070-9784-xx) and Wander Analyst 5.0 PC software (Tektronix part number 063-2955-xx) for TDEV/MTIE analysis. This PC application software is bundled with Option 14 - Jitter/Wander.
- The *CTS 850 SDH/PDH Test Set Service Manual* (Tektronix part number 070-9991-xx) provides information on maintaining and servicing your instrument to the module level

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Introduction

This manual contains all the information needed for periodic maintenance of the CTS 850 Test Set. Further, it contains all information for repair to the board or module level. This means that the procedures, diagrams, and other troubleshooting aids help isolate failures to a specific module, rather than to components of that module. Once a failure is isolated, replace the module with a replacement or exchange module obtained form Tektronix.

All modules are listed in the *Mechanical Parts List* section. To isolate a failure to a board or module, use the fault isolation procedures found in the *Maintenance* section. To remove and replace any failed board or module, follow the instructions in *Removal and Replacement Procedures*, also found in *Maintenance*.

Service Offerings

Tektronix provides service to cover repair under warranty. Other services are available that can provide a cost-effective answer to your service needs.

Whether providing warranty repair service or any of the other services listed below, Tektronix service technicians, trained on Tektronix products, are best equipped to service your CTS 850 test set. Tektronix technicians are apprised of the latest information on improvements to the product as well as the latest product options.

Warranty Repair Service

Tektronix technicians provide warranty service at most Tektronix service locations worldwide. (The warranty appears after the title page and copyright page in this manual.) Your Tektronix product catalog lists all service locations worldwide.

Repair Service

The following services can be purchased to tailor repair of your CTS 850 test set to fit your requirements.

Depot Service. Tektronix offers single per-incident repair and annual maintenance agreements that provide repair of the test unit.

Of these services, the annual maintenance agreement offers a particularly cost-effective approach to service for many owners of the test set. Such agreements can be purchased to span several years.

Self Service

Tektronix supports repair to the module level by offering a *Module Exchange* program.

Module Exchange. This service reduces downtime for repair by allowing you to exchange most modules for remanufactured ones. Tektronix ships you an updated and tested exchange module from the Beaverton, Oregon service center. Each module comes with a 90-day service warranty.

For More Information. Contact your local Tektronix service center or sales engineer for more information on any of the repair or adjustment services previously described.

Before You Begin

This manual is for servicing the CTS 850 Test Set. To prevent injury to yourself or damage to the instrument, do the following tasks before you attempt service:

- Read the *Safety Summaries* found at the beginning of this manual
- Read *Service Offerings* in this section

When using this manual to service your CTS 850 test set, be sure to heed all warnings, cautions, and notes.

Specifications

This section begins with a brief description of the CTS850 Test Set. Following the description, the section contains a complete listing of the instrument specification.

The organization of this section is as follows:

- Environmental Specifications (Table 1-1)
- Physical Specifications (Table 1-2)
- General Specifications (Table 1-3)
- Option 38 - PDH Tributary Specifications (Table 1-4)
- Option 14 - Jitter/Wander Specifications (Tables 1-5 through 1-8)
- Certifications and Compliance (Table 1-9)

Product Description

The CTS850 Test Set is a rugged, portable test set designed for installing and maintaining telecommunications networks. The CTS850 test set features the following capabilities (options are required for some features):

⇒ STM-0, STM-1, and STM-4 Transmit and Receive

⇒ STM-16 Transmit and Receive (when used with Tektronix ST2400)

⇒ VC4-4c Concatenated Payload Testing

⇒ 2, 8, 34, and 140 Mbit/s PDH Mux/Demux

⇒ Complete Jitter and Wander tests at Equipped Line Rates from 2 Mbit/s to 622 Mbit/s in one option – includes the Wander Analyst Application Software for TDEV/MTIE Analysis

⇒ Performance Monitoring per G.821, G.826, and M.2100; Pointer analysis and sequences per G.783

⇒ Full-band Jitter and Wander measurements to 0.1 Hz with variable high-pass cutoff frequencies

⇒ SDH/PDH Defect Generation and analysis

⇒ Manipulation of K1/K2 bytes for MPS/APS testing

⇒ Field-replaceable 1310 and 1550 nm optical interfaces

⇒ Autoscan with graphical display of signal format and payload

⇒ Histogram results, correlate alarms, errors, and events to 1s resolution

⇒ Pass/fail tests saved and recalled via floppy disk

Guide to the Specifications

This section contains the complete specifications for the CTS 850 Test Set.

All specifications are warranted unless they are designated *typical*. Warranted characteristics that are directly checked by a procedure contained in the *Performance Verification* section of this manual are marked with a n symbol.

If the characteristic is noted as *typical*, the characteristic is not warranted. Typical characteristics describe typical or average performance and provide useful reference information.

Performance Conditions

The electrical characteristics found in these tables apply when the CTS has been adjusted at an ambient temperature between +20° C and +30° C, has been warmed up for at least 20 minutes, and is being operated at an ambient temperature between 0° C and +50° C (unless otherwise noted).

Table 1-1: Environmental Specifications

Characteristic	Description
Temperature	Operating: 0° C to +40° C Non-operating: -40° C to +70° C
Altitude	Operating: Up to 4,572 m (15,000 ft) Non-operating: Up to 12,192 m (40,000 ft)
Humidity	Operating: 2 hours or less: Up to 95%, relative humidity at or below +40°C Continuous: Up to 90%,relative humidity at or below 30°C
Transportation Handling	Qualifies under National Safe Transit Association 1s Pre–shipment Test; 1A–B–1.

Table 1-2: Physical Characteristics

Characteristic	Description
Dimensions	Height: 165 mm (6.5 in) 191 mm (7.5 in) with accessory pouch Width: 362 mm (14.25 in) 564 mm (22.2 in) with handle extended Depth: 490 mm (19.25 in) with front cover
Weight	Net: Approximately 8.7 kg (19.3 lb) Shipping: Approximately 14.1 kg (31 lb)
Power Requirements	Source Power: AC Line Voltage Ranges:100v to 132v,180v to 250v *Line Voltage* *Line Frequency* 100 V to 132 V 50/60 Hz 180 V to 250 V 40 to 60 Hz 100 V to 132 V 400 Hz Maximum current: 6 A_{RMS}

Table 1-3: General CTS850 Specifications

Characteristic	Description
SDH Generator Output	
Electrical Output	
Data Rates	STM–0: 51.84 Mb/s STM–1: 155.52 Mb/s
Data Formats	STM–0E: B3ZS STM–1E: CMI
Signal Level at Transmit Output	STM–0E: ±1.0 Vpk ±10% into 75 Ω STM–0E (-6dB) STM-0E output attenuated with 6 dB cable loss(-12.7 dB √f characteristic cable) STM–1E : ±0.5 Vpk ±10% into 75 Ω STM–1E (-6dB) STM-0E output attentuated with 6 dB cable loss(-12.7 dB √f characteristic cable)
Pulse Shape at Transmit Output	Meets ITU–T G.703 Pulse Masks
Return Loss	>15 dB
Connectors	Unbalanced BNC, 75 Ω to ground Option 11 - 1.6/5.6, 75 Ω to ground
Optical Output	
Data Rates	STM–0: 51.84 Mb/s STM–1: 155.52 Mb/s STM–4: 622.08 Mb/s
Optical Module Options	Opt. 01, Electrical only, STM-0/1E Opt. 03, 1310 nm, IR, STM–0/1 Opt. 04, 1310 nm, IR, STM–0/1/4 Opt. 05, 1550 nm, LR, STM–0/1/4 Opt. 06, 1310/1550 nm, STM-0/1/4
Signal Level & Wavelength	-10 dBm, typical, 1310 nm, (Opt. 03, 04, 06) 0 dBm, typical, 1550 nm, (Opt. 05, 06)
Pulse Shape	Meets ITU–T G.957 Eye Pattern Masks
Wavelength	1308 nm, typical (Opt. 03, 04, 06) 1550 nm, typical (Opt. 05, 06)
Spectral Width	≤ 4 nm rms, 1310 nm (Opt. 03, 04, 06) ≤ 1 nm rms, 1550 nm (Opt. 05, 06)
Laser Classification	Class 1 laser, complies with 21 CFR 1040.10 and 1040.11, complies with IEC 825, Section 9.4
Connectors	User selectable when ordering: Opt. 31: FC-PC Opt. 32: ST Opt. 33: SC Opt. 34: DIN Other connector types- consult factory

Table 1-3: General CTS850 Specifications (Continued)

Characteristic	Description
SDH Signal Structure	
Payload Channel (AU)	Concatenated VC4-4c signal in STM-4: One active AU-4 in STM–1 One active AU-4 in STM-4 (The other 3 channels are unequipped) One active AU-3 in STM–0
Unequipped Payload	C2 byte is set to 00 Bulk fill set to 00
SDH Internal Pattern Generator	
Patterns Bulk Fill in a selected AU channel (AU-3 or AU-4)	Bulk Fill in a selected AU channel (AU-3 or AU-4): PRBS: 2^9-1, 2^{15}-1, 2^{20}-1, 2^{23}-1; All 1s, All 0s, 8–bit programmable word. PRBS patterns may be inverted. RSOH Orderwire - E1 RSOH User Byte - F1 MSOH Orderwire - E2 POH User Byte - F2 D1-D3 -- DCC D4-D12 -- DCC
Errors Single or Continuous rate	Single or Continuous Rate: RS BIP B1: STM0: 1.0e-3 to 1.0e-10 STM1: 1.0e-4 to 1.0e-10 STM4: 1.0e-5 to 1.0e-10 MS BIP B2: STM0: 1.0e-3 to 1.0e-10 STM1/4:1.0e-4 to 1.0e-10 Path BIP B3: STM0: 1.0e-3 to 1.0e-10 STM1/4:1.0e-4 to 1.0e-10 HP-REI G1: STM0: 1.0e-3 to 1.0e-10 STM1/4:1.0e-4 to 1.0e-10 Payload (Pattern Bit Error): 1.0e-3 to 1.0e-10
Alarms	Defects & Anomalies: MS-AIS,MS-RDI,AU-AIS,HP-RDI Failures: LOS, LOF, AU-LOP
SDH Transmitter Clock	
Internal Clock	Accuracy: ±4.6 ppm, for instrument calibrated within 36-months
External Clock Reference	Rates: 2.048 Mb/s ± 50 ppm 2.048 MHz ± 50 ppm 1.544 Mb/s ± 50 ppm Input: Unbalanced, 75 Ω, BNC connector, G.703 signal format

Table 1-3: General CTS850 Specifications (Continued)

Characteristic	Description
Recovered Clock	Loop timing: Clock is recovered from received signal
Transmit Line Frequency Offset rate	±100 ppm of nominal line rate, resolution 0.1 ppm
SDH Receiver Input	
Electrical Input	
Data Rates	STM–0: 51.84 Mb/s ±100 ppm STM–1: 155.52 Mb/s ±100 ppm
Data Formats	STM–0E: B3ZS STM–1E: CMI
Signal Sensitivity/ Equalization	STM–0E: 0.5 Vpk min to 1.2 Vpk max STM–0E -6 dB: 0.25 Vpk min to 0.6 Vpk max *-6dB cable loss @25Mhz(-12.7dB √f characteristic cable)* STM–0E -12dB: 0.125 Vpk min to 0.35 Vpk max *-12dB cable loss @25Mhz(-12.7dB √f characteristic cable)* STM–0E Monitor: 20 dB of flat loss below -6 dB STM–1E: 0.35 Vpk min to 0.6 Vpk max STM–1E -6 dB[3]: 0.35 Vpk min to 0.6 Vpk max *-6dB cable loss @25Mhz(-12.7dB √f characteristic cable)* STM–1E -12dB[4]: 0.07 Vpk min to 0.3 Vpk max *-12dB cable loss @25Mhz(-12.7dB √f characteristic cable)* STM–1E Monitor: 26 dB of flat loss below STM1-E level
Signal Level Display	Readout: Electrical signal level in mV
Return Loss	>15 dB
Connectors	Standard: Unbalanced BNC, 75 Ω to ground Option 12: 1.6/5.6, 75 Ω to ground
SDH Optical Input	
Data Rates	STM–0: 51.84 Mb/s (±100 ppm) STM–1: 155.52 Mb/s (±100 ppm) STM–4: 622.08 Mb/s (±100 ppm)
Maximum Input Power	-7 dBm: Opt. 05 and 06 include a 10 dB attenuator for use at 1550 nm
Operating Wavelength	1310 nm and 1550 nm: 1100 nm to 1570 nm operating range
Signal Sensitivity	-28 dBm for BER $<10^{-10}$
Optical Power Meter Accuracy	±2 dBm, typical For input power in a range of -30 dBm to -6 dBm Resolution: 0.1 dBm
Connectors	User selectable when ordering - Option 31: FC-PC; Option 32: ST; Option 33: SC; Option 34: DIN. Other connector types – consult factory.
Through Mode	Monitors a selected channel while passing the signal through unchanged (both electrically and optically)

Table 1-3: General CTS850 Specifications (Continued)

Characteristic	Description
Section Overhead	
Access	Set overhead bytes to any value from binary 00000000 to 11111111: A1, A2, J0, E1, F1, D1-D3, K1, K2, D4-D12, S1, M1, E2 View all Section Overhead bytes Clear text decode of S1 message byte provided per G.707
Add/Drop	Orderwire Access to E1 or E2 byte from RJ-11 jack. Insert data from the Overhead Add/Drop connector into the Section DCC, Line DCC, E1, E2 or F1 user byte. Drops data from the Section DCC, Line DCC, E1, E2, or F1 user byte out to the Overhead Add/Drop connector. PRBS evalution is provided internally for bytes E1, E2, F1, F2, D1-D3, D4-D12.
K1 and K2 (APS)	Set the APS Bytes, K1 and K2, to any code defined in ITU-G.783 Annex A or ANSI T1.105A Selectable by clear text for all Span and Ring messages
Path Overhead	
Access	Set Path Overhead bytes to any value from binary 00000000 to 11111111: C2, G1 (bits 5-7 only), F2, H4 (bits 1-6 only), F3, K3, N1 View all Path Overhead bytes Clear text decode of C2 signal label per ITU-G.707
Add/Drop	Insert data from the Overhead Add/Drop connector into the F2 user byte PRBS can be used via F2 internally
Trace Bytes J2, J1, J0	J2 LP-Trace: User-defined 16-byte sequence with CRC7 J1 HP-Trace: VC4 Overhead 16-byte with CRC-64 formats J0 RS-Trace: User-defined 64-byte sequence or 16-byte with CRC only
Pointer Movement	
Single	Single pointer justification
Burst	Bursts of two to eight pointer justifications spaced four frames apart. All adjustments within a given burst are in the same direction. Subsequent bursts are in alternating directions
Continuous	Pointer justifications occur continuously at a predetermined rate in an incrementing, decrementing, or alternating direction. Rate between movements: 2 ms to 10 s, with a resolution of 1 ms.
Set to Value	Set to a new location with or without the NDF being set. Range is 0 to 1023 (783 - 1023 are illegal locations).

Table 1-3: General CTS850 Specifications (Continued)

Characteristic	Description
Pointer Test Sequences	AU Pointer sequences available: G.783(a) Single Alternating G.783(b) Regular or Double G.783(c) Regular plus Missing G.783(d) Double Alternating G.783(e) Single G.783(f) Burst G.783(g1) Periodic 87-3 G.783(g2) Periodic 87-3 With Add G.783(g3) Periodic 87-3 With Cancel G.783(h1) Periodic G.783(h2) Periodic with Add G.783(h3) Periodic with Cancel Phase Transient Pointer Adjustment Burst
Pointer Direction	Positive or Negative
Initialization Period	On or Off - Thirty second burst of 1 pointer per second in the same direction as the selected test, per ITU-T G.783
Cool Down Period	On or Off - This will last at least 60 seconds for an integral number of complete sequences,per ITU-T G.783
SDH Measurements	
SDH Anomalies	Error Count, Error Rate, and Errored Seconds for: B1, B2, B3, Payload, MS–REI, HP–REI
Network Defects (Seconds)	LOS, LOP, LSS (Pattern Loss), CTS Loss of AC Power
SDH Defects (Seconds)	MS-AIS, MS-RDI, AU-AIS, HP-RDI, TU-AIS, LP-RDI, AU-LOP, RS-TIM, HP-TIM
AU Pointer Measurements	Loss Seconds, NDF Seconds, Illegal Seconds, +Ve Justification Count, -VE Justification Count, Illegal Count, NDF Count, Pointer Value
G.826 Analysis	RS B1: Seconds and ratio Error Blocks, ES, SES, UAS: Background Block Errors MS B2 & HP-REI: Seconds and ratio Error Blocks, ES, SES, UAS, CSES Periods: Background Block Errors Path B3 & LP-REI: Seconds and ratio Error Blocks, ES, SES, UAS, CSES Periods: Background Block Errors
G.821 Analysis	Pattern Bit Seconds and % of total time Error–Count, ES, DM, SES, UAS, EFS
SDH Standards Compliance	SDH Framing: G.707 SDH Multiplexing: G.707 SDH Optical Interfaces: G.957 SDH Electrical Interfaces: G.703 SDH Jitter Tolerance: G.825 and G.958 SDH Pointer Sequences: G.783 SDH Error Analysis: G.826 and G.821 SDH Test Patterns: O.181, O.150, and O.151

Table 1-3: General CTS850 Specifications (Continued)

Characteristic	Description
LEDs	
SDH Status Indicators	LOS, LOF, OOF, LOP, MS-AIS, MS-RDI, AU-AIS, HP-RDI, Signal Present, Pattern Lock, LSS, Error, Pointer Adjust
SDH Histograms	
Error Count	General: B1, B2, B3, MS–REI, HP–REI, Pattern Bit, Pointer Jitter
SDH Defects (On/Off)	LOS, OOF, LOF, AU–LOP, MS–AIS, AU-RDI, Path-AIS, Path-RDI, Pattern Loss, Loss of Power
SDH Pointers	AU Pointer Value, Pointer Justification
PDH and TU LEDs	
PDH and TU Status Indicators	TU-AIS, LP-RDI, PDH AIS, PDH RAI
Histograms for PDH & TU	
Error Count	General: E1 Anomalies, TU-BIP, LP–REI, Pattern Bit, Pointer Jitter
PDH & TU Defects (On/Off)	LOS, LOF, PDH-AIS, PDH-RAI, TU–LOP, TU–AIS, TU–RDI, TU-LOM, Pattern Loss, Loss of Power
TU Pointers	TU Pointer Value, Pointer Justification
Measurement Utilities	
Measurement Control	Manual Start/Stop Timed: 1 s to 99 days with 1 s resolution Continuous
Histogram Display Resolution	High: 1 sec (displays 1 hour with 1 sec resolution) Normal: 1 min, 5 min, 15 min, 1.2 hours (displays 3 hours with 1 min resolution) Low: 15 min, 60 min, 4 hrs, 12 hrs (displays 45 days with 15 min resolution)
Result Logging	All measurements are recorded with start/stop time & date. Current and previous results (totalized and graphical) are stored in memory. Both graphical and totalized results can be stored on disk.
Utilities	
TroubleScan	Scans all measurement results for key violations
AutoScan	AutoScan to incoming signal (rate, mapping, framing and pattern). Identifies incoming signal and presents graphical display of AU and TU structure. Identifies TU signal status by showing TU number, equipped versus unequipped, alarms, and pattern.
Stored Setups	5 front panel setups in memory 200 front panel setups per disk

Table 1-3: General CTS850 Specifications (Continued)

Characteristic	Description
Pass/Fail Tests	Predefined Pass/Fail Tests can be created, stored and executed 200 Pass/Fail test setups per disk
Add/Drop Interface for Data Communication Channels and User Channels	A DB–37 female connector provides the interface to an external protocol analyzer. Clock and data signals are differential TTL, conform to V.11 specifications, and are also compatible with single–ended TTL signals. Add/Drop: D1-D3, D4-D12, F1, F2, E1, E2 Connector: 37 Pin DIN (DTE and DCE) RJ11-style handset jack for analog access to E1/E2 bytes
Triggering	Pulse at start of each SDH frame, (Tx and Rx), Connector: 37 Pin DIN
Disk Drive	3.5 inch, 1.44 MB, DOS-compatible Stored Setups and Pass/Fail Tests
Printer	Optional printer in pouch (thermal): HC 411 Printer support: Epson, HP Thinkjet, ASCII text Serial Printer Port: V.24 Printer Formats: Print to disk, BMP format, Interleaf format, Encapsulated PostScript, ASCII text
Computer Interface	IEEE–488.2 interface RS–232–C interface (DB9 connector)
Help Mode	Online task–oriented help
Display	Type: 7-inch diagonal CRT, green phosphor Resolution: 640 by 480 pixels VGA output: 15-pin connector

Table 1-4: CTS 850 Opt. 38 PDH Tributaries Specifications

Characteristic	Description
2 Mb/s, 8 Mb/s, 34 Mb/s, 140 Mb/s Generator	The data format can be built upon the pattern generator framed or unframed output at the PDH line/mapping rate, or upon multiple layers of user-configurable sub-multiplexing. A specific hierarchy or tributaries can be selected and filled with a background pattern.
Electrical Output	
Data Rates	2 Mb/s: 2.048 Mb/s ± 100ppm 8 Mb/s: 8.448 Mb/s ± 100ppm 34 Mb/s: 34.368 Mb/s ± 100ppm 140 Mb/s: 139.264 Mb/s ± 100ppm
Formats	2 Mb/s, 8 Mb/s, 34 Mb/s: HDB3, AMI 140 Mb/s: CMI
Signal Level	2 Mb/s: 3 Vpk ± 0.3 V into 120 Ω 2 Mb/s: 2.37 Vpk ± 0.237 V into 75 Ω 8 Mb/s: 2.37 Vpk ± 0.237 V into 75 Ω 34 Mb/s: 1 Vpk ± 0.1 V into 75 Ω 140 Mb/s: 1 Vp-p ± 0.1 V into 75 Ω
Pulse Shape	Meets ITU–T G.703 Pulse Masks
Connectors	2 Mb/s: 3-pin Siemens 120 Ω 2 Mb/s, 8 Mb/s, 34 Mb/s, 140 Mb/s: BNC 75 Ω
PDH Output	Data Source: 2 Mb/s: Internal Pattern Generator Configured from N x 64kbit/s Drop from SDH TU12 Drop from demuxed 8 Mb/s and above From 2 Mb/s input (through mode) 8 Mb/s: Internal Pattern Generator Muxed up from 2 Mb/s From 8 Mb/s input (through mode) 34 Mb/s: Internal Pattern Generator Muxed up from 8 Mb/s Drop from SDH TU3 Drop from demuxed 140 Mb/s From 34 Mb/s input (through mode) 140 Mb/s: Internal Pattern Generator Muxed up from 34 Mb/s Drop from SDH VC4 From 140 Mb/s input (through mode)

Table 1-4: CTS 850 Opt. 38 PDH Tributaries Specifications (continued)

Characteristic	Description
2 Mb/s, 8 Mb/s, 34 Mb/s, 140 Mb/s Internal Pattern Generator	
Framing	2 Mb/s: Unframed N x 64kbits/s (with starting TS & range) FAS (31 channel) FAS + CRC4 (31 channel) FAS + MFAS (30 channel) FAS + CRC4 + MFAS (30 channel) (G.704, G.737, G.732) 8 Mb/s: Unframed FAS (G.742) 34 Mb/s: Unframed FAS (G.751) 140 Mb/s: Unframed FAS (G.751)
Patterns (for PDH Testing Line/Mapped)	Active Channel Patterns in selected measurement channels. N x 64 Kbit/s: PRBS 2^9-1 per O.153 PRBS 2^{11}-1 per O.152 PRBS 2^{15}-1 per O.151 PRBS 2^{20}-1 per O.153 PRBS 2^{23}-1; per O.151 All the above may be inverted All 1s All 0s TS Idle 1020 Hz audio tone 2,8,34,140 Mbit/s: PRBS 2^9-1 per O.153 PRBS 2^{11}-1 per O.152 PRBS 2^{15}-1 per O.151 PRBS 2^{20}-1 per O.153 PRBS 2^{23}-1; per O.151 All the above may be inverted All 1s All 0s Alternating 1/0 1 in 8 8, 16, 24-bit User-selectable pattern Fill Patterns in background non-measurement channels. N x 64 Kbit/s: TS Idle (55 H) 2 Mb/s : PRBS 2^{15}-1 All 1s All 0s Alternating 1/0 8,34,140 Mbit/s: PRBS 2^{15}-1 per O.151 PRBS 2^{20}-1 per O.153 PRBS 2^{23}-1; per O.151 All the above may be inverted All 1s All 0s Alternating 1/0

Table 1-4: CTS 850 Opt. 38 PDH Tributaries Specifications (continued)

Characteristic	Description
Errors	Single, Continuous, Burst (all are mutually exclusive and effective on active channels only)
Error Type	CRC (2 Mb/s only): minimum rate 1.0E-8 Maximum rate 1.0E-4 Frame Burst (available on any ONE enabled multiplexed level) (2,8,34,140 Mb/s): N<M<1000 where: M=frame count N= consecutive FAS Error count *Pattern Bit* - first line is Payload Pattern bit at active pattern's rate; Second line is *Line Code*: 64 kb/s: Min: 1.0E-6, Max: 1.0E-2, *Line Code: not applicable* 2 Mb/s: Min: 1.0E-8, Max: 1.0E-2 *Line Code: min. 1.0E-8, max. 1.0E-3* 8 Mb/s: Min: 1.0E-9, Max: 1.0E-2 *Line Code:* min. 1.0E-10, max. 1.0E-3 34 Mb/s: Min: 1.0E-9, Max: 1.0E-2 *Line Code:* min. 1.0E-10, max. 1.0E-3 140 Mb/s:Min: 1.0E-9 , Max: 1.0E-2 *Line Code: not applicable*
Alarm Insertion	2 Mb/s: AIS, RAI - NFAS bit 3=1 8 Mb/s: AIS, RAI - NFAS bit 11=1 34 Mb/s: AIS, RAI - NFAS bit 11=1 140 Mb/s: AIS, RAI - NFAS bit 13=1
TU12/TU3/VC4 Mapping	Mapping Signal Source for TU12, TU3, and VC4
Internal Generator	Received Signal: 2 Mb/s : 2 Mb/s 34 Mb/s: 2, 34 Mb/s 140 Mb/s: 2, 34, 140 Mb/s Mapping mode: floating asynchronous
TU12 Active Map Channel Selection	Allows selection of any one of 63 TU channels, or all TU-12s simultaneously, Remaining 62 TU channels are background
TU3 Active Map Channel Selection	Allows selection of any one of 3 TU channels, or all TU-3s simultaneously, Remaining 2 TU channels are background
140 Mb/s Active Map Channel Selection	Into selected STM–1 VC4
TU12 Background Channel Content	When internal 2 Mb/s or 34 Mb/s generator is used: PRBS: 2^{15}-1 or Idle pattern (11010101) when external source is used: PRBS: 2^{15}-1
TU Background Channel Framing	All unframed unless All TUs
TU3 Background Channel Content	When internal 34 Mb/s generator is used: VC3 is a Bulk-filled pattern, Valid Pointer & BIP. Bulk-fill data is 01, 02,& 03 for TU3 #1, #2,& #3.

Table 1-4: CTS 850 Opt. 38 PDH Tributaries Specifications (continued)

Characteristic	Description
TU Errors (Single or Continuous)	Single or Continuous TU12 BIP-2, TU3 BIP-8, LP-REI
TU Alarms and Failures	TU AIS: LP-RDI TU Loss of Pointer TU Loss of Multiframe
Transmitter Clock	
Transmit Line Frequency Offset	Frequency offset rate: 2 Mb/s: ±100 ppm of nominal line rate 8 Mb/s: ±100 ppm of nominal line rate 34 Mb/s: ±100 ppm of nominal line rate 140 Mb/s: ±100 ppm of nominal line rate Resolution: 0.1 ppm
2 Mb/s, 8 Mb/s, 34 Mb/s, 140 Mb/s Receiver	
Electrical Input	
Data Rates	2 Mb/s (2.048 Mb/s): ±150 ppm 34 Mb/s (34.368 Mb/s): ±150 ppm 140 Mb/s (139.264 Mb/s): ±150 ppm
Formats	2 Mb/s: HDB3, AMI 8 Mb/s: HDB3, AMI 34 Mb/s: HDB3, AMI 140 Mb/s: CMI
Impedance	2 Mb/s: 120 Ω balanced 2 Mb/s Bridged: 1 kΩ balanced 2 Mb/s, 34 Mb/s, 140 Mb/s: 75 Ω unbalanced
PDH Receive Signal Level	ITU-T G.703 nominal pulse and signal level: Normal: Auto equalization of root-f cable loss to ITU-T G.703 limits *2Mb/s and 8Mb/s root-f cable loss = 6 dB max* 2 Mb/s Bridged: Auto equalization of root-f cable loss to ITU-T G.703 limits *34Mb/s and 140Mb/s root-f cable loss = 12 dB max* Protected Monitor Point -20dB:-15 to –23dB flat loss *2Mb/s Bridged only specified for 120 Ω balanced cable* Protected Monitor Point -30dB:-23 to -31dB flat loss, except at 140Mb/s: -23 to –30dB flat loss, typical
Connectors	2 Mb/s: 3-pin Siemens 120 Ω 2 Mb/s, 8 Mb/s, 34 Mb/s, 140 Mb/s: BNC 75 Ω

Table 1-4: CTS 850 Opt. 38 PDH Tributaries Specifications (continued)

Characteristic	Description
2 Mb/s, 8 Mb/s, 34 Mb/s 140 Mb/s Internal Pattern Receiver	
Pattern Receiver Source	N/Mx64 kbit/s & 2 Mb/s: 2 Mb/s External SDH TU12 Drop Demuxed 8 Mb/s and above 8 Mb/s: 8 Mb/s External Demuxed 34 Mb/s 34 Mb/s: 34 Mb/s External SDH TU3 Drop Demuxed 140 Mb/s 140 Mb/s: 140 Mb/s External SDH VC4 Drop
Framing	N/Mx64kbit/s & 2 Mb/s: Unframed FAS (31 channel) FAS plus CRC4 (31 channel) FAS plus MFAS (30 channel) FAS plus CRC4 plus MFAS (30 channel) (G.704, G.737, G.732) 8 Mb/s: Unframed FAS (G.737) 34 Mb/s: Unframed FAS (G.751) 140 Mb/s: Unframed FAS (G.751) CAS (Signaling in TS 16) Bits displayed: a,b,c,d VFchannel 1 to 30 Value displayed: 1 or 0
TU12/TU3/VC4 Demapping	
Demapping TU12, TU3 and VC4	Signal Drop to: Internal Receiver: 2 Mb/s 34 Mb/s 140 Mb/s External Signal Output: 2 Mb/s 34 Mb/s 140 Mb/s
Demapping mode	Floating Asynchronous TU12 Active Demap Channel Selection: Allows selection of any one of 63 TU channels TU3 Active Demap Channel Selection: Allows selection of any one of three TU channels 140 Mb/s Active Demap Channel from selected STM–1 VC4

Table 1-4: CTS 850 Opt. 38 PDH Tributaries Specifications (continued)

Characteristic	Description
TU Path Overhead	
TU12 Path Overhead Access, bits 5-7 only	V5 control (----xxxx-) Set Path Overhead bytes to any value from binary 00000000 to 11111111: N2 and K4 View all TU Path Overhead bytes
TU3 Path Overhead Access	Set Path Overhead bytes to any value from binary 00000000 to 11111111: (set G1 bits 5-7 only) C2, F3, K3, N1 (H4 bits 1-6 only) View all TU Path Overhead bytes
TU3 Path Trace Byte J1	Send user–defined 15-bytes & CRC sequence or set to all “ space” characters View Path Trace J1
TU12 Path Trace Byte J2	Send user–defined 16–byte sequence or set to Null (00000000), View Path Trace J2
TU Pointer Measurement	
TU Pointer Interaction	TU12, TU3, or AU4, but not at the same time Single: Single pointer justification (increment or decrement) Burst: Bursts of two to eight pointer justifications spaced four multi–frames apart. All adjustments within a given burst are in the same direction. Subsequent bursts are in alternating directions. Continuous: Pointer justifications occur continuously at a predetermined rate in an incrementing, decrementing, or alternating direction. Rate between movements: 48 ms to 10 s, with a resolution of 1 ms.
Set to Value	Set to a new location with or without the NDF being set. TU12 Range is from 0 to 1023 (140 - 1023 are illegal locations). TU3 Range is from 0 to 1023 (783 - 1023 are illegal locations).
TU Pointer sequences available	G.783(a) Single Alternating G.783(b) Regular + Double G.783(c) Regular + Missing G.783(d) Double Alternating G.783(e) Single G.783(f) Burst G.783(g1) Periodic 87-3 G.783(g2) Periodic 87-3 With Add G.783(g3) Periodic 87-3 With Cancel G.783(h1) Periodic G.783(h2) Periodic with Add G.783(h3) Periodic with Cancel

Table 1-4: CTS 850 Opt. 38 PDH Tributaries Specifications (continued)

Characteristic	Description
Phase Transient Pointer Adjustment Burst	TU–3 Periodic 85-5 TU–3 Periodic 85-5 With Add TU–3 Periodic 85-5 With Cancel TU–12 Periodic 35-1 TU–12 Periodic 35-1 With Add TU–12 Periodic 35-1 With Cancel
Pointer Direction	Positive or Negative Initialization Period: On or Off, thirty second burst of 1 pointer per second in the same direction as the selected test Cool Down Period: On or Off, this will last at least 60 seconds
PDH & TU Measurements	
PDH Error Count, Error Rate and Error seconds	FAS CRC–4 (2 Mb/s only) Pattern Bit
TU Error Count, Error Rate and Error seconds	TU12 BIP-2: TU3 BIP–8 TU12 RDI: TU3 RDI
PDH Alarm and Failure Seconds	AIS: RDI Loss of Sync Sequence (LSS) Loss of Frame (FAS) Loss of Signal
TU Alarm and Failure Seconds	TU AIS TU RDI TU Loss of Pointer TU Loss of Multiframe
TU Pointer Measurements	Seconds: LOP, Illegal pointers, NDF Count: Illegal pointers, Positive justifications, Negative justifications
G.826 Analysis for TUs	TU12 BIP–2 & RDI Seconds and ratio Error Blocks, ES, SES, UAS, CSES background block Errors RDI-count, RDI-ES, RDI-UAS, RDI-EFS
TU3 BIP–8 & RDI	Seconds and ratio Error Blocks, ES, SES, UAS, background block errors RDI-count, RDI-ES, RDI-UAS, RDI-EFS
G.821 Analysis for PDH	PDH Frame & CRC–4 Errors, Seconds, and % of total time Error–Count, ES, SES, UAS, EFS, DM
Payload (Pattern Bit Errors)	Seconds and percent of total time Error–Count, ES, SES, UAS, EFS, DM
M.2100 Analysis for PDH	In-service seconds and percent of total time: Error–Count, ES, SES, UAS, EFS Out-of-service seconds and percent of total time: Error–Count, ES, SES, UAS, EFS

Table 1-4: CTS 850 Opt. 38 PDH Tributaries Specifications (continued)

Characteristic	Description
G.826 Analysis for PDH *(Within channel(s) under test at all enabled MUX levels)*	In-service for selected rate: ES, %ES, SES, %SES, UAS, %UAS For remote selected rate: ES, %ES, SES, %SES, UAS, %UAS, PUAS, %PUAS
PDH Standards Compliance	PDH Mapping/Demapping: G.707 PDH Line Interfaces: G.703 PDH Jitter Tolerance: G.823 PDH Error Analysis: G.821, G.826, M.2100 PRBS Test Patterns: O.151, O.152, O.153 Monitor Mode Levels: G.772 PDH Framing: G.704, G.732, G.732, G.737, G.742, G.751

Table 1-5: CTS 850 Opt. 14 Jitter and Wander Specifications

Characteristic	Description
Jitter Generator (requires Option 14)	Meets or exceeds the requirements of ITU-T G.823, G.825, O.171, O.17s (draft)
Jittered Line Output	Sinusoidal modulation of transmit clock freq., applicable to any SDH or PDH data rate, except 8 Mbit/s (E2).
Modulation Range	Modulation is selectable up to specific limits, which depend upon the rate. Refer to Table 1-4.
Amplitude Accuracy	622Mb/s: ± 5% ± 0.06 UI All other rates: ± 5% ± 0.03 UI
Amplitude Resolution	0.01 UI, nominal
Frequency Accuracy	below 1.00 KHz: ± 1% above 1.00 KHz: ± 5 ppm
Frequency Resolution	3 decimal places
Jittered Clock Output	Operates in addition to the jittered line output when selected. Compliant with G.703 2048kHz synchronization interface specifications.
Output Level(typical)	0.8 V_{p-p} all rates, AC-coupled, unbalanced 75 Ω termination
2 MHz G.703 output	Compliant with G.703 2048 KHz synchronization interface specifications
Nominal Clock Rates	2 MHz, 34 MHz, 52 MHz, 140 MHz, 155 MHz, or 622 MHz. Can be set independently of transmit line rate
Connector	Rear–panel, unbalanced 75 Ω BNC
Jitter and Wander Analysis for SDH/PDH	Peak–to–peak or RMS jitter measurement of the Clock or Line input. Meets or exceeds the requirements of ITU–T G.783, G.823, G.825, G.958, O.171, and O.17s (draft).
Jitter Measurements	Peak–to–peak Jitter (UI), Positive Peak Jitter (UI), Negative Peak Jitter (UI), Jitter Hit Seconds, Jitter Unlocked Seconds, RMS (UI)

Table 1-5: CTS 850 Opt. 14 Jitter and Wander Specifications (continued)

Characteristic	Description
Timing Quality	Video-related measurements: Pointer Event Seconds, Current Frequency Drift Rate (ppm/sec), Maximum Frequency Drift Rate (ppm/sec)
Normal and Extended Jitter Measurement Resolution and Range	Normal Resolution: 0.005 UI. Resolution is 0.1 UI for Fullband (0.1 Hz Highpass). Resolution for RMS is 0.001 UI_{RMS} Extended Resolution: 0.01UI,except fullband 0.1 Hz, 0.1UI Range: See Table 1-6
Fixed Error Noise with Clock (typical)	For peak-to-peak measurement specifications in UI_{p-p}, refer to Table 1-7
Fixed Error with PRBS Data Signal (typical)	For peak-to-peak measurement specifications in UI_{p-p}, refer to Table 1-7
Jitter Measurement Accuracy	Jitter measurement accuracy is a function of the modulation frequency and the highpass filter chosen. Measured jitter frequency response is expressed by the equation: $\sqrt{\frac{1}{1+\left(\frac{f_{LC}}{f}\right)^2}} \times \sqrt{\frac{1}{1+\left(\frac{f}{f_{UC}}\right)^6}}$ where, f_{LC} = lower cutoff frequency f_{UC} = high frequency cutoff (defined below) Pass-band is from f_{LC} to f_{UC}. Uncertainity = ± 5A ± fixed error, where A is the actual jitter at the point.
Measurement Frequency Response	Measurement filters meet the requirements of ITU–T G.783, G.823, G.825, G.958, and O.17 (draft). Lower cutoff (high pass): first order (-20 dB/decade). Upper cutoff (low pass): third order (-60 dB/decade). Filter response at cutoff frequencies is -3 dB ± 1 dB, except for 2 Mb/s 100KHz cutoff where response is 0 to –3dB.
Wideband Filter (-3 dB)	2 Mb/s: 20 Hz to 100 kHz 34 Mb/s 100 Hz to 800 kHz 140 Mb/s 200 Hz to 3.5 MHz STM–0E: 100 Hz to 400 kHz STM–1E: 500 Hz to 1.3 MHz STM–1: 500 Hz to 1.3 MHz STM–4: 1 kHz to 5 MHz
Highband Filter (-3 dB)	2 Mb/s: 18 kHz to 100 kHz (Low Q) 2 Mb/s: 700 Hz to 100 KHz (High Q) 34 Mb/s: 10 kHz to 800 kHz 140 Mb/s 10 kHz to 3.5 MHz STM–0E: 20 kHz to 400 kHz STM–1E: 65 kHz to 1.3 MHz STM–1: 65 kHz to 1.3 MHz STM–4: 250 kHz to 5 MHz

Table 1-5: CTS 850 Opt. 14 Jitter and Wander Specifications (continued)

Characteristic	Description
Fullband Filter (-3 dB)	Lower –3dB frequency is user selectable to 0.1 Hz, 1 Hz, or 10 Hz. 2 Mb/s: 10 Hz to 100 kHz 34 Mb/s 10 Hz to 800 kHz 140 Mb/s 10 Hz to 3.5 MHz STM–0E: 10 Hz to 400 kHz STM–1E: 10 Hz to 1.3 MHz STM–1: 10 Hz to 1.3 MHz STM–4: 10 Hz to 5 MHz
RMS Filter (-3 dB)	2 Mb/s: 12 kHz to 100 kHz 34 Mb/s: 12 kHz to 800 kHz 140 Mb/s: 12 kHz to 3.5 MHz STM–0E: 12 kHz to 400 kHz STM–1E: 12 kHz to 1.3 MHz STM–1: 12 kHz to 1.3 MHz STM–4: 12 kHz to 5 MHz
Jitter Clock Input	Input to measure jitter on a clock signal.
Nominal Clock Rates	Any supported SDH or PDH rate, except 8 Mbit/s (E2). Rate is independent of the receive line rate.
Frequency Tolerance	Nominal rate ±100 ppm
Input Amplitude	0.4 V_{p-p} minimum, 1.5 V_{p-p} maximum
Connector	Rear–panel, unbalanced 75 Ω BNC
Analog Jitter Output	Demodulated jitter from the receiver. The output is filtered by any measurement filters selected.
Connector	Rear–panel, 50 Ω BNC
Sensitivity (typical)	Normal measurement range: 100 mV/UI Extended measurement range: 2.65 mV/UI
Output Level (typical)	± 1V, centered at 0 V ± 100 mV
Accuracy	± 5%, in addition to measurement inaccuracy
Lock Time	Wideband, Highband, or Fullband (10 Hz) Highpass Filter: <5 s 1.0 Hz Highpass Filter: <30 s fullband 0.1 Hz Highpass Filter: <60 s fullband
Wander Measurements	According to ITU-T G.813, G.812, ETS300 462-n. Sample Rate: 50 Hz
Peak-to-Peak Measurement	Range: 48.8 ms Noise: ±5 ns for observation periods ≤100 seconds Accuracy: 1% ± noise Bandwidth: 0 Hz to 10 Hz Resolution: 1 ns

Table 1-5: CTS 850 Opt. 14 Jitter and Wander Specifications (continued)

Characteristic	Description
TIE Measurement	Range: 48.8 ms Noise: ±5 ns for observation periods ≤100 seconds Accuracy: 1% ± noise Bandwidth: 0 Hz to 10 Hz Resolution: 1 ns
Frequency Measurement	Resolution: 1 Hz absolute (0.01 ppm relative) Accuracy: ±0.1 ppm with respect to source clock
Frequency Drift Rate	Range: 0 to 867.480 ppm/sec Accuracy: <1% ± 0.01 ppm/sec Bandwidth 0 Hz to 0.5 Hz Resolution: 0.001 ppm/sec

Table 1-6: CTS 850 Opt. 14 Modulation Range for Jitter Generator Specifications

Amplitude Scale (UI_{p-p})	A0	A1	A2	A3
All rates	100,000	10	3	1

Frequency Scale (Hz)	F0	F1	F2	F3	F4	F5
2 Mb/s rate	12 µHz	30 mHz	300 Hz	9 KHz	33 KHz	100 KHz
34 Mb/s rate	12 µHz	30 mHz	300 Hz	10 KHz	270 KHz	800 KHz
140 Mb/s rate	12 µHz	30 mHz	300 Hz	20 KHz	1.2 MHz	3.5 MHz
52 Mb/s rate	12 µHz	30 mHz	300 Hz	10 KHz	130 KHz	400 KHz
155 Mb/s rate	12 µHz	30 mHz	300 Hz	35 KHz	430 KHz	1.3 MHz
622 Mb/s rate	12 µHz	30 mHz	300 Hz	125 KHz	1.7 MHz	5.0 MHz

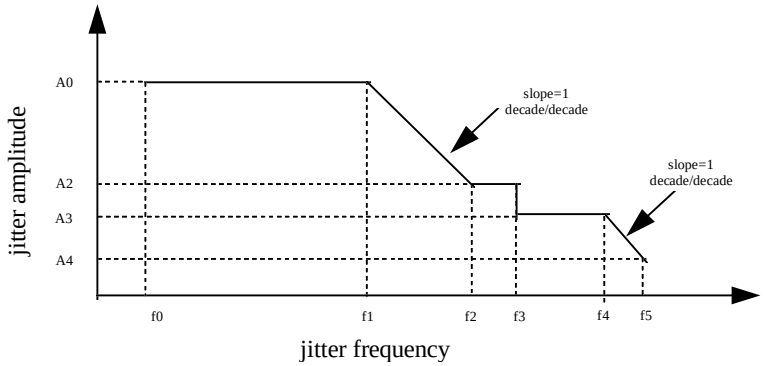


Table 1-7: CTS 850 Opt. 14 Normal & Extended Jitter Measurement Range Specifications

Amplitude Scale (UI_{p-p})	**A1**	**A2**	**A3**	**A4**
2 Mb/s rate	200 UI	10 UI	6 UI	0.5 UI
34 Mb/s rate	200 UI	10 UI	6 UI	0.5 UI
140 Mb/s rate	200 UI	10 UI	6 UI	0.5 UI
52 Mb/s rate	200 UI	10 UI	6 UI	0.5 UI
155 Mb/s rate	200 UI	10 UI	6 UI	0.4 UI
622 Mb/s rate	200 UI	10 UI	6 UI	0.3 UI

Frequency Scale (Hz)	**F1 (Hz)**	**F2 (Hz)**	**F3 (Hz)**	**F4 (KHz)**	**F5 (KHz)**	**F6 (KHz)**	**F7**
2 Mb/s rate	0.1	15	300	1.9	3.2	38.4	100 KHz
34 Mb/s rate	0.1	15	300	8	13.3	160	800 KHz
140 Mb/s rate	0.1	15	300	16	26.7	320	3.5 MHz
52 Mb/s rate	0.1	15	300	16	26.7	320	400 KHz
155 Mb/s rate	0.1	15	300	16	26.7	320	1.3 MHz
622 Mb/s rate	0.1	15	300	40	68	1330	5.0 MHz

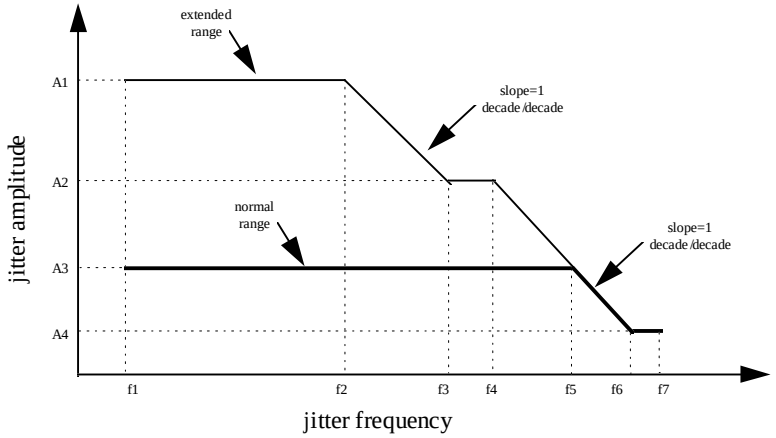


Table 1-8: CTS 850 Opt. 14 Fixed Error with Clock and Data Specifications

Fixed Error Noise with Clock						Fixed Error with PRBS Data Signal					
			Fullband						Fullband		
Rate (Mb/s)	Highband	Wideband	10 Hz	1 Hz	0.1 Hz	Rate (Mb/s)	Highband	Wideband	10 Hz	1 Hz	0.1 Hz
2	0.02	0.03	≤0.1	≤0.2	≤0.70	2	0.035	0.035	≤0.1	≤0.2	≤0.7
34	0.02	0.03	≤0.1	≤0.2	≤0.70	34	0.035	0.035	≤0.1	≤0.2	≤0.7
140	0.02	0.03	≤0.1	≤0.2	≤0.70	140	0.035	0.035	≤0.1	≤0.2	≤0.7
52	0.02	0.03	≤0.1	≤0.2	≤0.70	52	0.035	0.035	≤0.1	≤0.2	≤0.7
155	0.02	0.03	≤0.1	≤0.2	≤0.70	155	0.035	0.035	≤0.1	≤0.2	≤0.7
622	0.05	0.06	≤0.1	≤0.75	≤1.00	622	0.06	0.07	≤0.1	≤0.75	≤1.00

For RMS measurements, ≤ 0.01UI_{RMS} at all rates.

Table 1-9: Certifications and compliance

Characteristic	Description
FCC Compliance	Emissions comply with FCC Code of Federal Regulations 47, Part 15, Subpart B, Class A Limits
EC Declaration of Conformity - EMC	Meets intent of Directive 89/336/EEC for Electromagnetic Compatibility. Compliance was demonstrated to the following specifications as listed in the Official Journal of the European Communities: EN 55011 EN 50082-1 AS/NZS 2064.1/2 IEC 801-2 IEC 801-3 IEC 801-4 IEC 801-5
EC Declaration of Conformity - Low Voltage	Compliance was demonstrated to the following specification as listed in the Official Journal of the European Communities: Low Voltage Directive 73/23/EEC, Amended by 93/68/EEC
Safety	Class: Class 1, as per IEC 1010-1, Annex H, grounded product. Compliance was demonstrated for: EN 61010-1 ANSI/ISA S82.02.01 IEC 1010-1 UL 3111-1 CAN/CSA–22.2 No. 1010.1 (Overvoltage CAT II per IEC 1010-1, Annex J)
Other Compliance	Pollution Degree: Degree 2 as defined in IEC 1010-1. Rated for indoor use only.

Installation

This section provides important information about installing the CTS850 Test Set.

Supplying Operating Power

WARNING. Read all information and heed all warnings in this subsection before connecting the CTS to a power source.

AC POWER SOURCE AND CONNECTION. The CTS operates from a single–phase power source. It has a three–wire power cord and a two–pole, three–terminal grounding type plug. Make sure that the correct plug is attached to the CTS before connecting to a power source. The voltage to ground (earth) from either pole of the power source must not exceed the maximum rated operating voltage, 250 V_{RMS}.

GROUNDING. This instrument is safety Class 1 equipment (IEC designation). All accessible conductive parts are directly connected through the grounding conductor of the power cord to the grounded (earthing) contact of the power plug.

The power-input plug must be inserted only in a mating receptacle with a grounding contact where earth ground has been verified by a qualified service person. Do not defeat the grounding connection. Any interruption of the grounding connection can create an electric shock hazard.

For electric shock protection, the grounding connection must be made before making connection to the instrument's input or output terminals.

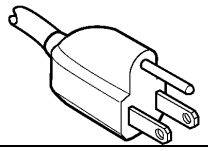
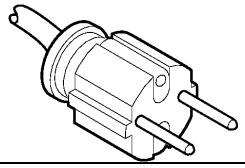
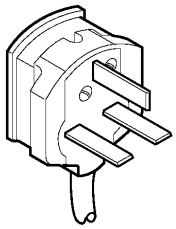
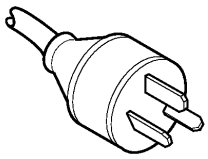
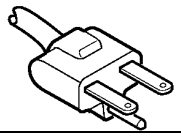
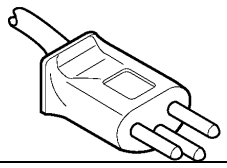
Power Cord Information

A power cord with appropriate plug configuration is supplied with each CTS. Table 2-1 gives the color–coding of the conductors in the power cord. If you require a power cord other than the one supplied, refer to Table 2-2, *Power Cord Options*.

Table 2-1: Power Cord Conductor Identification

Conductor	Color	Alternate Color
Ungrounded (Line)	Brown	Black
Grounded (Neutral)	Light Blue	White
Grounded (Earthing)	Green/Yellow	Green

Table 2-2: Power Cord Options

Plug Configuration	Normal Usage	Option Number	Part Number
	North America 115 V	Standard	161–0066–00
	Europe 230 V	A1	161–0066–09
	United Kingdom 230 V	A2	161–0066–10
	Australia 230 V	A3	161–0066–11
	North America 230 V	A4	161–0066–12
	Switzerland 230 V	A5	161–0154–00

Operating Voltage

The *Specification* section lists line voltage ranges and their associated line frequency ranges over which the CTS operates. See the *Power Requirements* specification for these ranges.

CAUTION. Before stepping the source line voltage from one range to a higher range, set the principal power switch (rear panel) to its OFF position. Failure to do so can damage the CTS.

Your CTS is equipped with one of two possible fuse types. Either type can be used throughout the line voltage and frequency ranges. These two fuses are not totally interchangeable because each requires a different fuse cap. The fuses and their caps are listed by part number in Section 10, *Mechanical Parts List.*

Memory Backup Power

Replaceable lithium batteries maintain internal memory modules to allow the CTS to retain the following data if you lose AC power: stored adjustment constants, saved setups, the current setup (instrument status), and test results from the last two tests.

These batteries have a shelf life of about five years. Partial or total loss of stored setups at power–on may indicate that the batteries need to be replaced.

Operating Environment

The following information describes environmental characteristics required for proper operation and long instrument life.

Operating Temperature

The CTS 850 Test Sets can be operated (without disk media) where the ambient air temperature is between -0° C and +40° C and can be stored (without disk media) in ambient temperatures from -40° C to +70° C. After storage at temperatures outside the operating limits, allow the chassis to stabilize at a safe operating temperature before applying power.

Ventilation Requirements

The CTS is cooled by air drawn in and exhausted through its cabinet side panels by an internal fan. To ensure proper cooling of the instrument, allow at least two inches clearance on both sides and $^3/_4$ inch on the bottom of the CTS. (The feet on the bottom of the CTS provide the required clearance when set on flat surfaces.) The top of the CTS does not require ventilation clearance.

CAUTION. If airflow is restricted, the CTS power supply may temporarily shut down.

Applying and Interrupting Power

Consider the following information when you power on or power off the instrument, or when power is interrupted due to an external power failure.

Powering On

At power–on, the CTS runs its power–on self test. If it passes, the CTS displays the message Internal diagnostics passed. If it fails, the CTS displays the message Internal diagnostics failed. See Section 6, *Maintenance*, for information on diagnostics and fault isolation.

Powering Off

Wait for the CTS to finish saving setups, pass/fail tests, or test results before turning off power. In general, do not power off the CTS during operations that involve saving data. If power is interrupted during a save operation, the saved data may be incomplete or corrupted.

Installed Options

The CTS may be equipped with one or more instrument options. These options are listed in the *Options* section. For further information and prices of CTS options and accessories, see your Tektronix Products catalog or contact your Tektronix Field Office.

Operating Information

This section provides an overview of CTS 850 operation, but covers only the features to service or verify performance of the test unit. For more details about test unit operation, refer to the *CTS 850 SDH/PDH User Manual* or the *CTS 850 Reference on CD*.

Front–Panel Controls, Indicators, and Connectors

Figures 2-1 and 2-2 identify the controls, indicators, and connectors located on the front panel of the CTS 850 SDH/PDH Test Set.

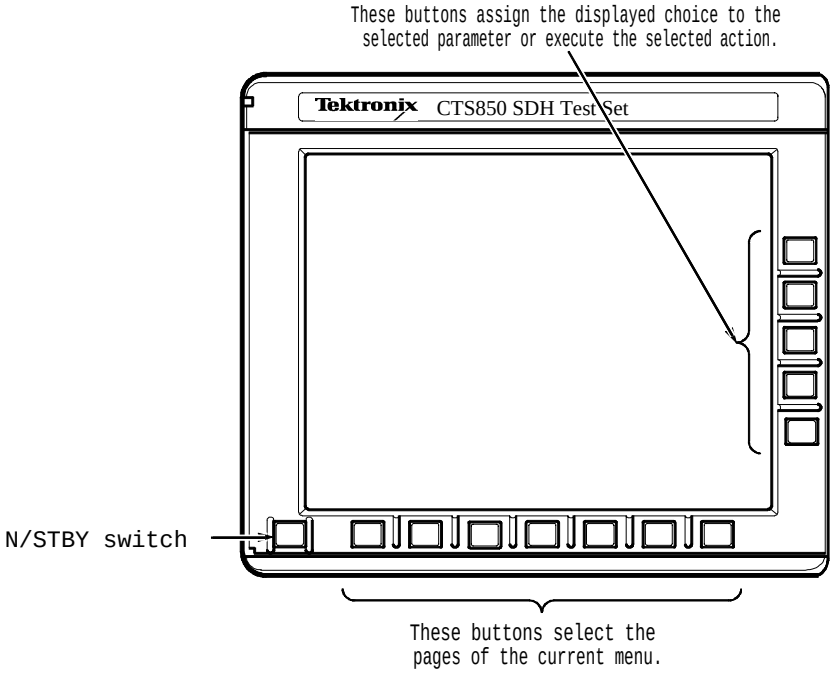


Figure 2-1: Controls Located around the Display

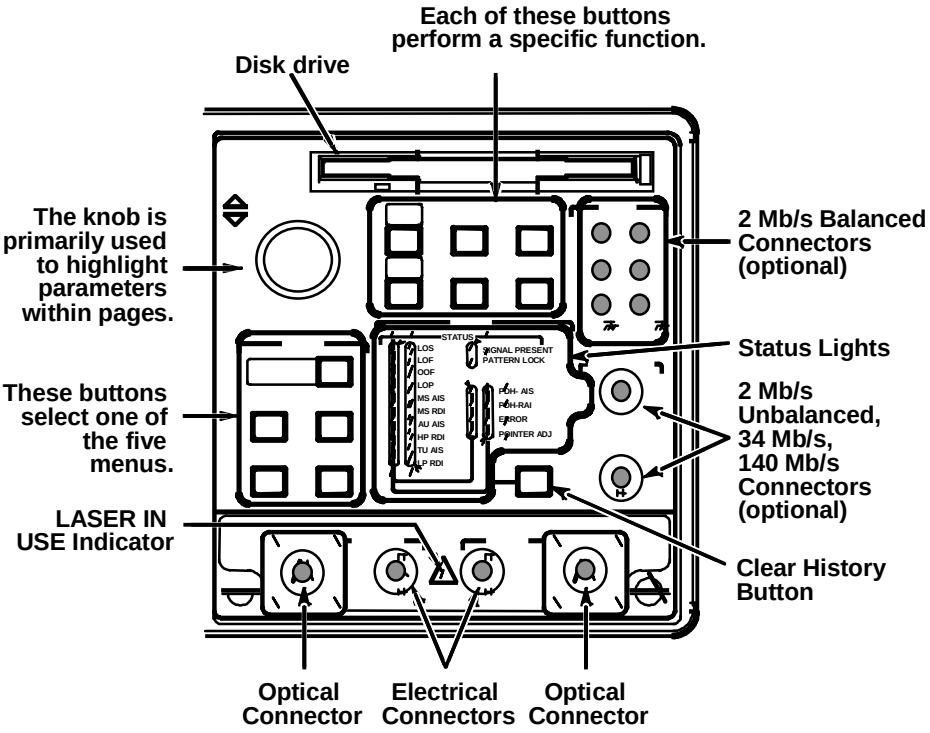


Figure 2-2: Front–Panel Controls, Indicators, and Connectors

Front–Panel Status Lights

The status lights make it easy to quickly determine the condition of the received signal. There are three types of front–panel status lights (see Figure 2-3).

- Green status lights. Green lights indicate whether a signal is present and whether the CTS850 has locked onto the signal.
- Red status lights. When a red status light is on, it means that the indicated event is occurring. When the red light is off, no event is occurring.
- Yellow history lights. Once an event has been detected, a yellow history light is turned on. The yellow history light shows that the associated event occurred at some time in the past. Yellow history lights remain on until you reset the event history by pressing the CLEAR HISTORY button, starting a new test, or changing the Receive Configuration settings (Receive Rate, Receive Patterns, etc.)

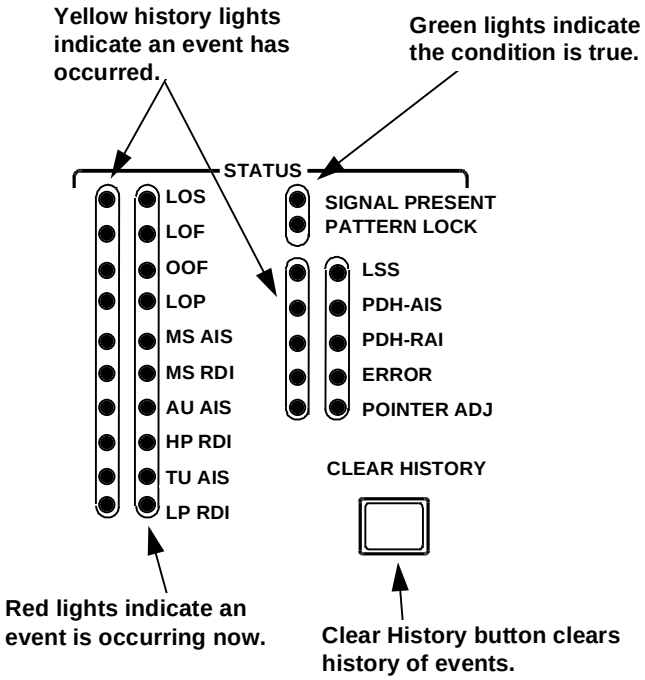


Figure 2-3: Status Lights

Reading the Display

There are several major areas that make up the CTS 850 display (see Figure 2-4). Figure 2-5 provides a guide to specific areas of the display.

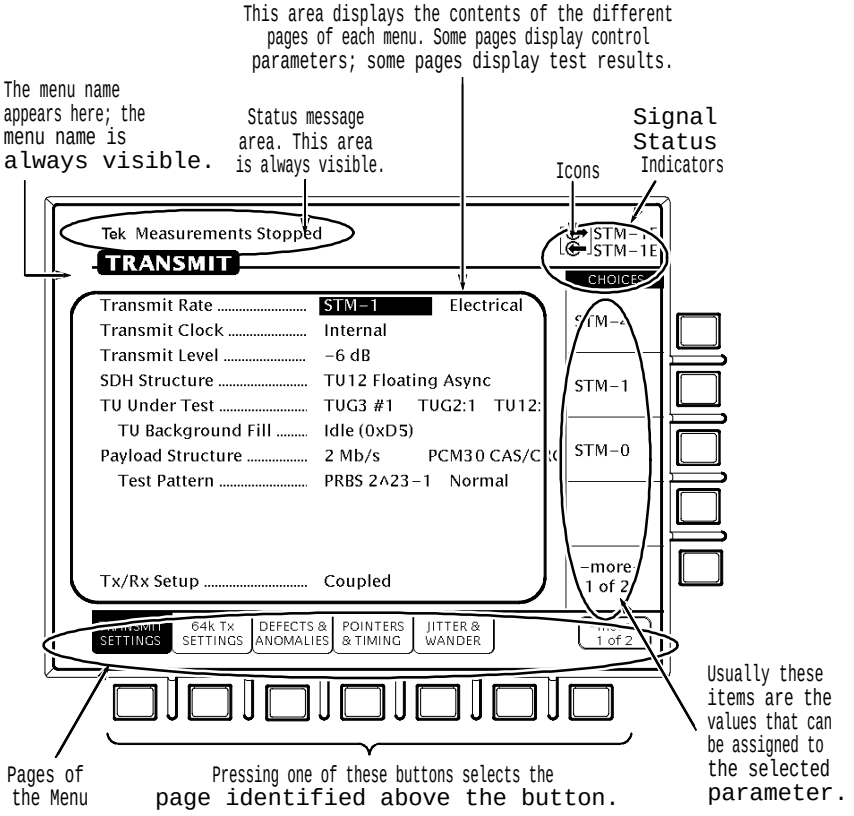


Figure 2-4: Major Areas of the Display

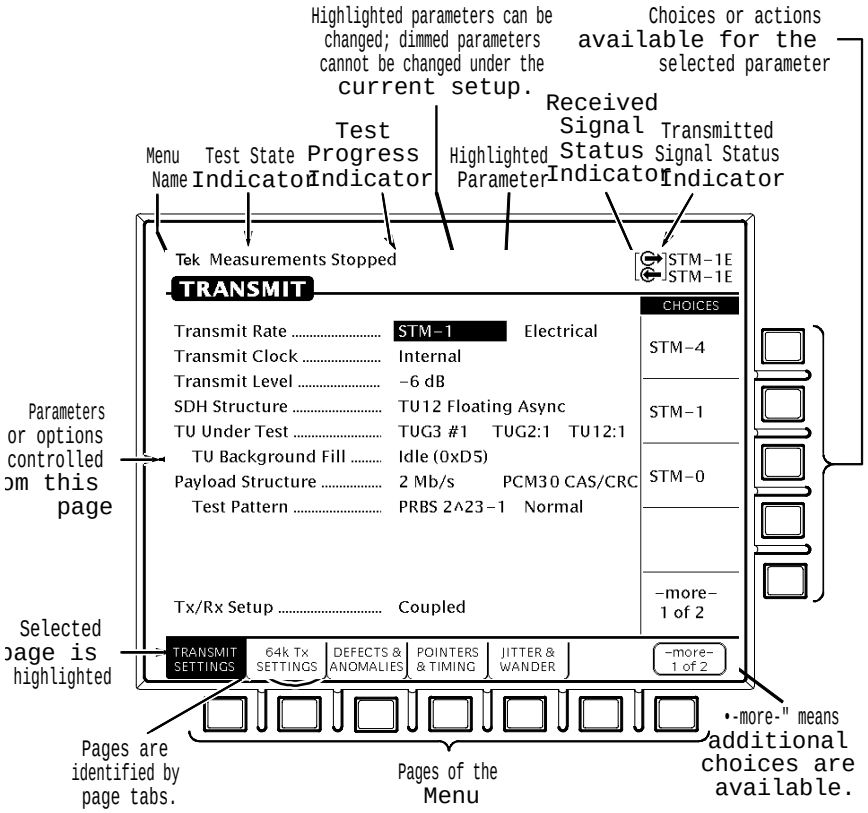


Figure 2-5: Specific Elements of the Display

The Basic Menu Structure

The CTS 850 is controlled primarily through its menu system. Though several controls are located on the front panel, such as INSERT ERROR, most functions are controlled from one of the five menus. Figure 2-6 shows the five menus.

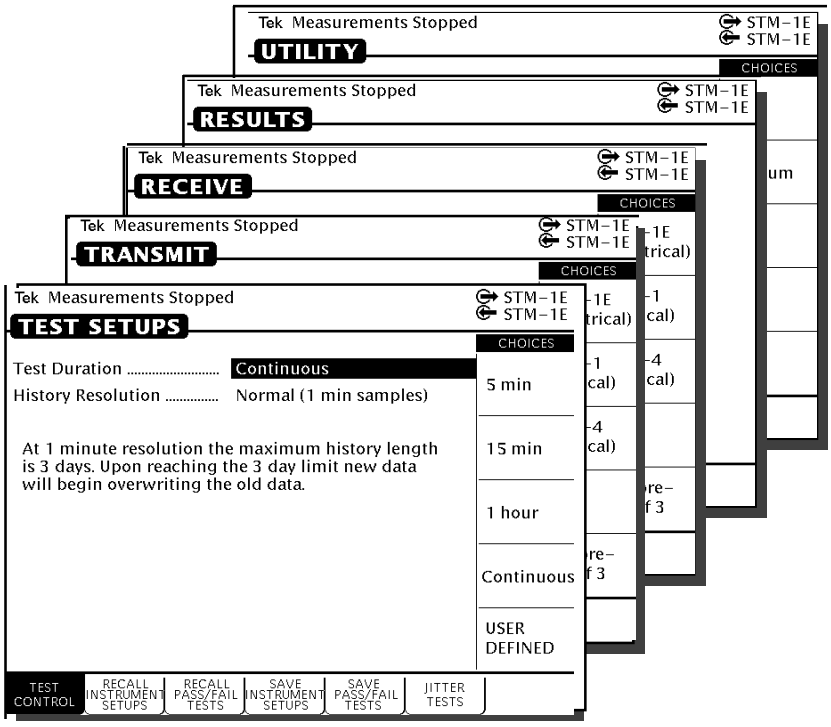


Figure 2-6: The Five Menus

What is a Menu?

A menu groups related functions together. For example, all settings that affect the signal transmitted by the CTS 850 are located in the TRANSMIT menu. Each menu is made up of pages. A page is identified by a page tab located at the bottom of the display (see Figure 2-7).

If the choice is not available, it is not displayed or it is not highlighted.

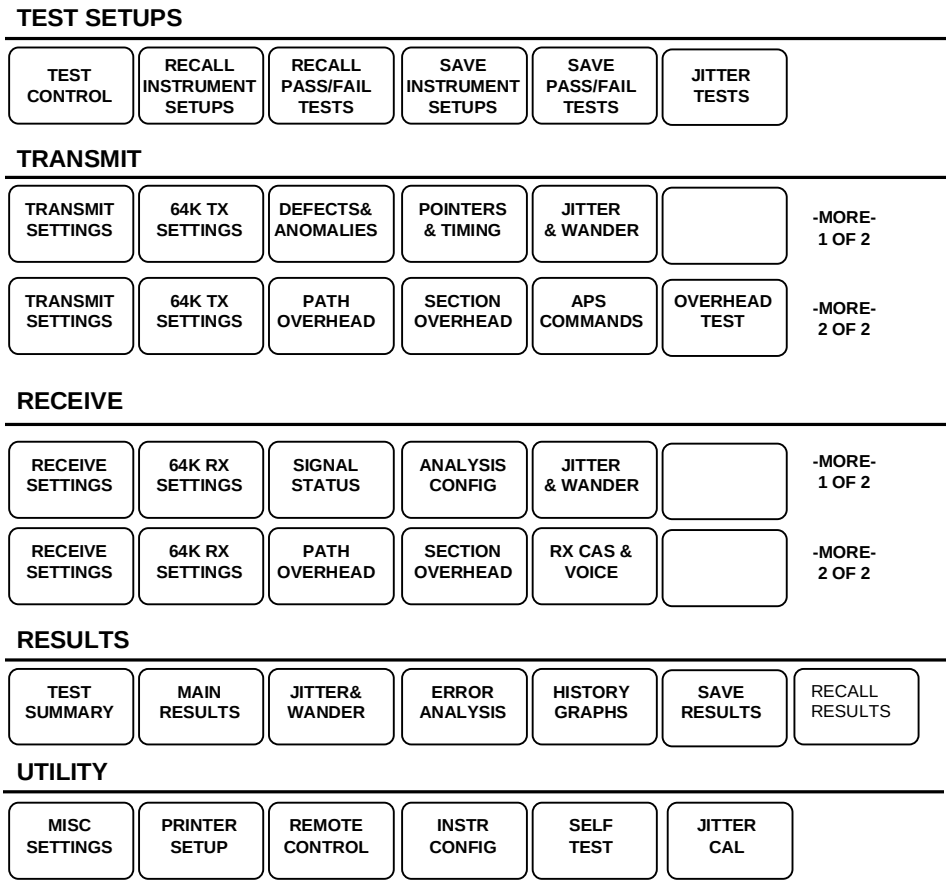


Figure 2-7: Menus and Pages

The CTS 850 always displays a menu. The name of the current menu is shown near the top of the display. To change to another menu, press a menu button on the front panel.

NOTE. The only time pressing a menu button does not change menus is when a dialog box is displayed or when you are entering a value for a parameter. You must first exit the dialog box or finish entering the value before you can change menus.

A page usually provides control over a related group of instrument functions or parameters. For example, the TRANSMIT SETTINGS page in the TRANSMIT menu controls the rate, format, and active channels of the signal transmitted by the CTS 850. However, some pages display information rather than provide control over settings; for example, the pages of the RESULTS menu display various test results.

Selecting Menus

To display a menu, press the button with the same on the front panel with the same name (see Figure 2-8).

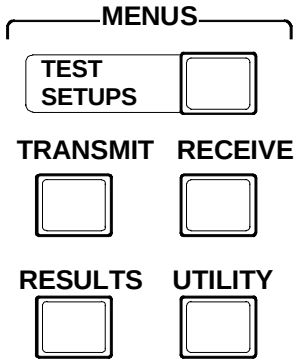


Figure 2-8: Menu Select Buttons

Connecting Signals

To connect signals to the CTS 850, use the electrical and optical connectors located at the bottom and right side of the front panel.

For optical connections, the CTS 850 accepts both single-mode and multimode fiber. For electrical connections, the CTS 850 accepts 75 Ohm coaxial cable with BNC connectors for SDH rate and @ Mb/s Unbalanced, 8 Mb/s, 34 Mb/s, and 140 Mb/s rates. The CTS 850 accepts Siemens connectors for 2 Mb/s Balanced signals.

Connecting Optical Signals

NOTE. The optical TRANSMIT output is produced by a Class 1 laser device. The output from a Class 1 laser is safe to view without special eye protection. However, because other optical signals in your environment may exceed the Class 1 limits, we recommend eye protection as a precaution.

To connect optical signals to the CTS 850:

1. Unscrew the dustcap that covers the optical port on the CTS 850.
2. Remove the dustcap (if present) covering the connector on the optical fiber.
3. Carefully insert the transmit end of the optical fiber into the **RECEIVE** port on the CTS 850. Line up the key on the optical fiber connector with the cutout on the optical port connector. Make sure that the optical fiber connector is fully inserted into the optical port.
4. Tighten the optical fiber connector so it does not accidentally come loose during use.

5. Carefully insert the receive end of the optical fiber into the **TRANSMIT** port on the CTS 850 line up key. Make sure that the optical fiber connector is fully inserted into the optical port.
6. Tighten the optical fiber connector so it does not accidentally come loose during use. Tighten the connectors only finger tight; do not use a tool to tighten the connectors.

CAUTION. To prevent damage to the optical port connectors and to keep them clean, always replace the dustcaps on the optical port connectors when not using the optical ports.

Connecting SDH Electrical Signals

To connect SDH electrical signals to the CTS 850:

1. Connect the transmit end of the cable to the **RECEIVE** connector on the CTS850.
2. Connect the receive end of the cable to the **TRANSMIT** connector on the CTS850.

Connecting PDH Electrical Signals

To connect electrical signals to the CTS 850:

1. Connect the transmit end of the cable to the **IN** connector for the appropriate rate on the CTS 850.
2. Connect the receive end of the cable to the **OUT** connector for the appropriate rate on the CTS 850.

Some procedures require several iterations of highlighting parameters and selecting choices. Some procedures may require more than one menu button or menu page selection as well.

Note: Use the buttons below the display to Select Menu Page. Use the rotary knob to Highlight Parameter. Use the buttons to the right of the display to Select Choice.

Rear–Panel Controls and Connectors

Each of the connectors on the rear panel is explained below (see Figure 2-9). For further detail, refer to the *CTS850 Test Set User manual*.

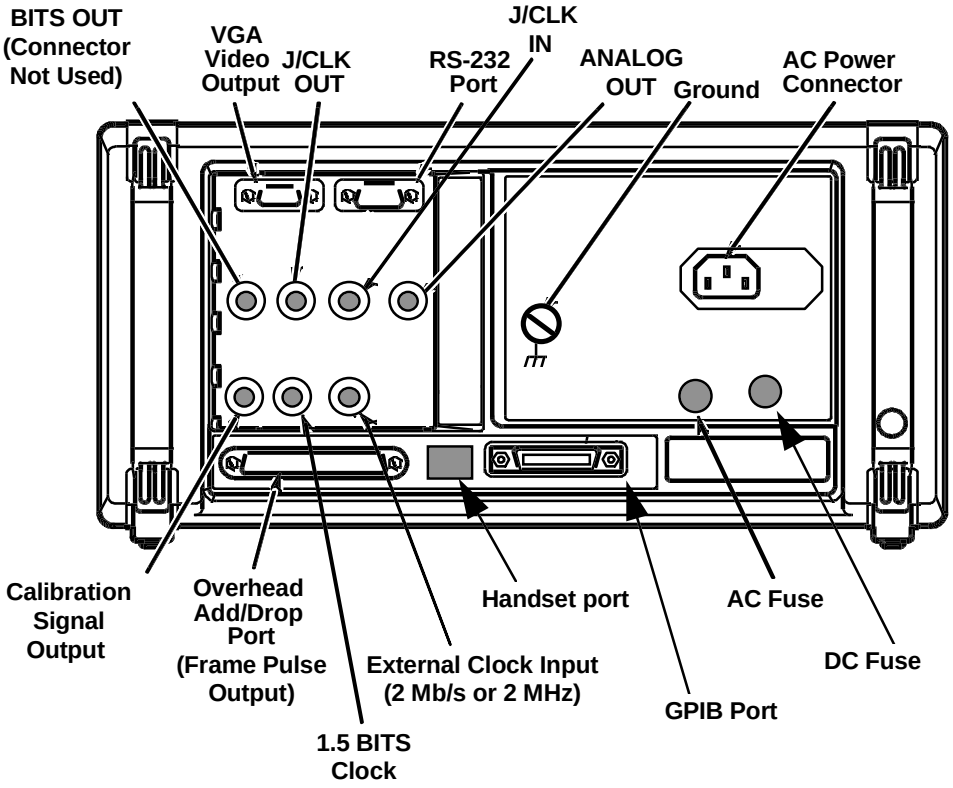


Figure 2-9: Rear–Panel Controls and Connectors

VGA Video Output

The CTS850 can drive an external IBM-compatible VGA monitor. There are no parameters to set in order to drive an external monitor. The output is monochrome (green only); the resolution is 640 pixels x 480 pixels.

GPIB Port

The GPIB (General Purpose Interface Bus) port is used for remote control of the CTS850. For detailed information on remote control of the CTS850, see the *CTS850 Test Set Programmer Manual*.

RS-232 Port

The rear panel RS-232 (male) connector is used to connect to printers and instrument controllers. Set the RS-232 parameters for printers on the PRINTER SETUP page of the UTILITY menu. Set the RS-232 parameters for instrument controllers on the REMOTE CONTROL page of the UTILITY menu. You can find more detailed information on remote control of the CTS850 in the *CTS850 Test Set Programmer Manual*.

Calibration Signal Output

The Calibration signal output is used for servicing the CTS850.

Overhead Add/Drop Port

The Overhead add/drop (female) connector is used to add/drop the section and line data communication channels (DCC) and the section and line user channels. The DCC and user channel add/drop functions are independent; for example, you can add a DCC while dropping a user channel. Only one DCC or user channel can be added or dropped at a time. The parameters for adding a DCC or a user channel are located on the SECTION OVERHEAD and PATH OVERHEAD pages of the TRANSMIT menu. The parameters for dropping a DCC or a user channel are located on the SECTION OVERHEAD and PATH OVERHEAD pages of the RECEIVE menu.

External Clock Input (2 Mb/s or 2 MHz) and 1.5 BITS Clock

To synchronize the CTS850 transmit clock with a 2 Mb/s or 2 MHz reference, connect a 2 Mb/s or 2 MHz reference to the External Clock Input connector. The 1.5 BITS clock can also be used to time the transmitter.

Handset Interface

The following handset interface specifications are compatible with an Audiosears handset (vendor part number 2600-A-00-JAFC-AAJ-05). This Audiosears handset uses a 2212 speaker (receiver) and a 2251 Amplified Electret microphone (transmitter). Other handsets with similar specification will also work. Handsets with non-amplified Electret (Standard) microphones may also be used.

Jitter Inputs and Outputs

If the CTS850 Test Set has the Jitter Test Option (Option 14) installed, four additional connectors are located on the rear panel in the JITTER/WANDER group. The connections in order from left to right are listed below. If measuring Jitter and/or Wander at line rates, use the regular connections on the front panel of the CTS850 Test Set.

BITS OUT (Connector – not used)

The BITS OUT connector is not used by the CTS850 Test Set.

J/CLK OUT

J/CLK OUT (jittered clock output) provides a clock line rate signal modulated by generated jitter. You can choose any SDH or PDH rate. In addition, the J/CLK OUT connector can provide a 2.048 MHz G.703 synchronization signal. Refer to the *CTS850 User Manual* for more information about controlling the signal type, rate, jitter, and frequency offset.

The J/CLK OUT connector is a 75 Ω BNC. The output is ECL compatible when terminated by 75 Ω.

J/CLK IN

J/CLK IN (jitter clock input) is an input you can use to measure the jitter on a MHz clock signal. The signal must be NRZ coded and at an SDH or PDH rate. Refer to the *CTS50 User Manual* for more information about setting the jitter measurement source and rate.

The J/CLK IN connector is a 75 Ω BNC. The input is AC coupled. Typical sensitivity is 0.4 V_{p-p}.

ANALOG OUT

The ANALOG OUT connector provides the demodulated jitter from the receiver as an analog waveform. An oscilloscope or spectrum analyzer may be used to analyze this waveform, as long as the limitations of the oscilloscope or spectrum analyzer in terms of this type of telecommunications information is realized.

The ANALOG OUT signal is not calibrated; the amplitude has low accuracy, but the spectral content is valid. The spectral content is dependent on the measurement filter you select. Refer to the CTS850 User Manual for more information about controlling the measurement range and filter.

The ANALOG OUT connector is a 75 Ω BNC. The signal level is typically ±1V or less and is centered at 0 V. Typical sensitivity is 125 mV/UI in normal mode and 3.5 mV/UI in extended mode.

Theory of Operation

This section describes the electrical operation of the CTS 850 Test Set. The description is based on the block diagram located in the *Diagrams* section of this manual, and gives an overall view of the module design. This description, together with the troubleshooting and diagnostics information in the *Maintenance* section, enable a qualified technician with the appropriate test equipment to isolate a problem to the faulty module.

Module Descriptions

As you read the following module descriptions, refer to the block diagram located in the *Diagrams* section.

Display/CPU

The Display/CPU board combines the functions of a display board and a CPU board. The functions include the video display interface, a disk drive interface, non-volatile RAM, and an interface to the Protocol boards.

The video display is standard VGA format. Text and graphics information is sent to the A26 Monitor assembly as a video signal. (Text and graphics are processed by different parts of the Display circuitry.) The Display circuitry also generates and sends vertical (VSYNC) and horizontal (HSYNC) sync signals to the A26 Monitor assembly. A VGA–compatible video output is available at the rear of the instrument.

The disk drive interface connects to the DOS–format floppy disk drive. All disk controller circuitry resides on the Display board.

The non-volatile RAM is 2 Mbytes of battery–backed RAM, which is used to store setup information.

The protocol board interface circuitry passes System Bus signals to the Protocol boards. Access to the protocol boards and the interface boards passes through the Display board.

The CPU coordinates all CTS activities (including the activities of the Front Panel Processor). The CPU is a 32 MHz 68020 which is interfaced to a PC–AT bus for communications with peripherals. The CPU also supports the I^2C bus for serial communications to peripherals. The CPU has 1 Mb dynamic RAM and 3 Mb of FLASH EPROM program storage. A clock/calendar is also included.

A02 Backplane

The A02 Backplane is the major wiring harness and power distribution point for the CTS. The A02 Backplane regulates the ±12 V supply, and provides it to boards plugged into the A02 Backplane. For the Protocol boards, the A02 Backplane supplies ±12 V through the cable harness, not the backplane.

Regulation for -5 V is done locally on boards requiring that voltage, rather than on the A02 Backplane. A –3.3 V DC/DC converter is mounted to the backplane for possible use with future options.

A04/A05 Plug-In Interface Module

The primary function of the Plug–In Interface Module is converting the optical and electrical standard signals to (and from) the TTL and ECL digital signals used by the Protocol Processor. Secondary functions are clock recovery for the 52 Mb/s rate and measuring received optical and electrical signal levels. The optical and electrical signal levels are returned as analog voltages. The Plug–In Interface Module also has an Active Signal Present line which is polled by the CPU.

Figure 3-1 is a block diagram of the Plug–In Interface Module. The following descriptions correspond to the functional blocks shown in the block diagram.

CPU Interface. The A03 CPU board communicates with the Plug–In Interface Module through three I^2C Bus registers (1–to–8 serial–to–parallel bus expanders). These registers, called the state setup registers, are responsible for the following functions:

- Register 0 is read–only and contains the board configuration, board version, and status of the Active Signal Present line.
- Register1 is read/write and controls the SONET/SDH signal interface and signal path.
- Register2 is read/write and controls the optical signal interface.

Receiver Rate Select. The Receiver Rate Select block controls the received signal path from the front–panel connectors to the protocol interface connector. The Receiver Rate Select block is controlled through the state setup registers.

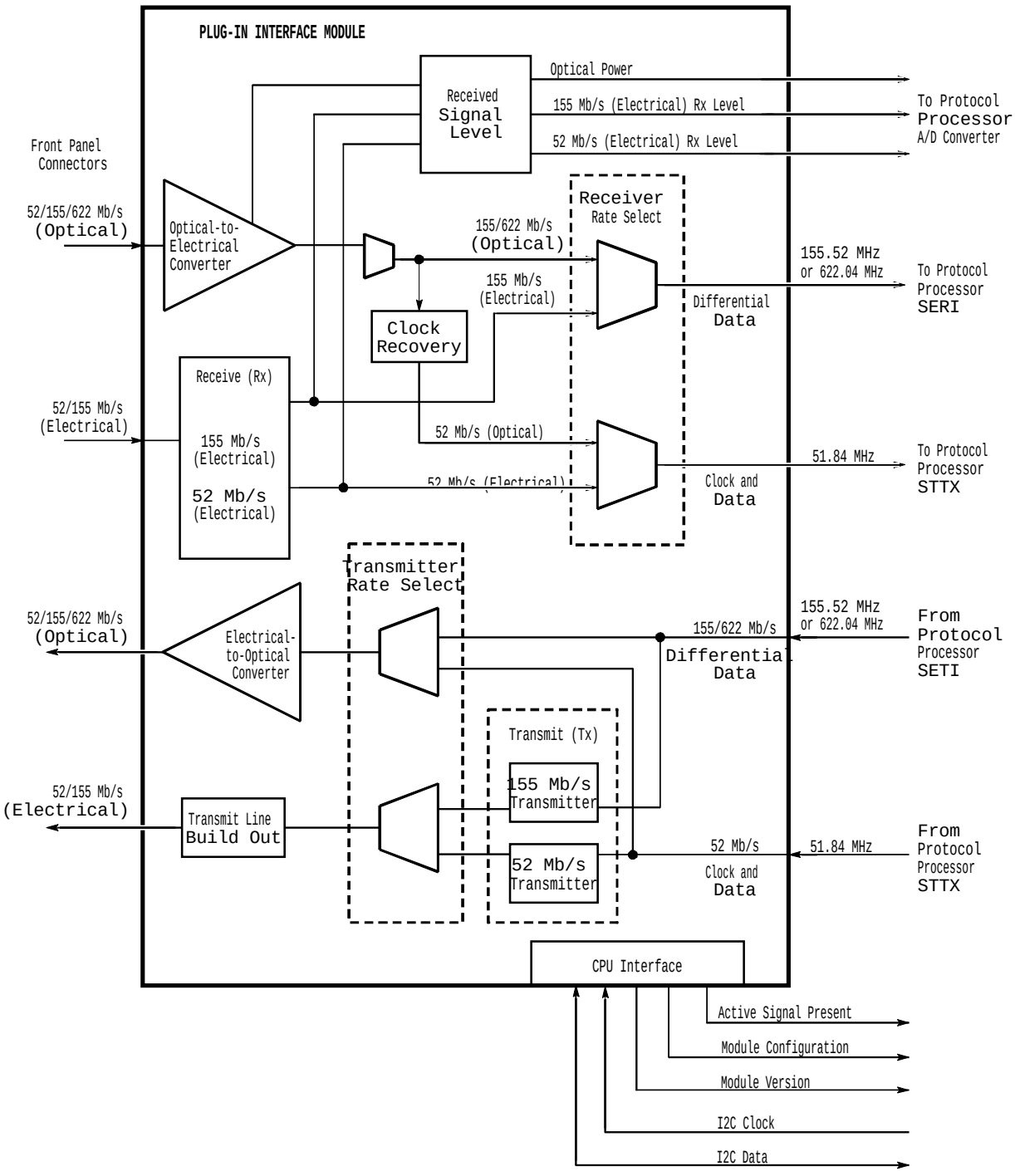


Figure 3-1: Plug–In Interface Module Functional Block Diagram

Receive (Rx). The Receive block contains the 52 Mb/s and 155 Mb/s receivers. This block also contains circuitry for detection of Active Signal Present.

The 52 Mb/s receiver performs amplification, equalization, clock recovery, data retiming, and B3ZS decoding. Note that equalization of frequency loss from the transmission cable is not automatic; it must be selected by the operator. The choices are cross–connect or low (maximum cable length). There is significant overlap in the response of the associated filters.

The 155 Mb/s receiver performs equalization and ECL conversion. No operator selections are necessary to set up the 155 Mb/s receiver. Equalization is automatic, performed by an active device.

Optical–to–Electrical Converter and Clock Recovery. The Optical–to–Electrical Converter block receives an optical signal and generates a corresponding differential ECL NRZ pulse train. It can receive 52 Mb/s, 155 Mb/s, and 622 Mb/s signal rates. The received 52 Mb/s signal undergoes further processing in the Clock Recovery block, making the signal compatible with the 52 Mb/s recovered signal format. The Clock Recovery block accepts the differential data stream and outputs a differential clock and retimed data streams, which are then level shifted to TTL levels.

Received Signal Level. Each of the receiver circuits has a peak voltage indicator or, in the case of optical signals, an average incoming power indicator.

Transmitter Rate Select. The Transmitter Rate Select block is controlled by means of the state setup registers (refer to page -2). This block controls the transmit signal path from the front connectors to the protocol interface connector.

This includes two groups of switches; relays to switch the outgoing analog signals, and multiplexers to switch digital data from the protocol board. The relay selects routing for the outgoing signal (to the 155 Mb/s transmitter or the 52 Mb/s transmitter), while the multiplexers select between the electrical and optical data options for the different clock rates.

Transmit (Tx). The Transmit block contains the 52 Mb/s and the 155 Mb/s transmitters.

The 52 Mb/s transmitter performs B3ZS encoding, amplification, and pulse shaping. The amplification must be selected by the operator. The choices are high or cross–connect.

The 155 Mb/s transmitter is more complicated. It has an active current source, a differential amplifier, and an all–pass network to allow matched termination at high and cross–connect outputs.

Transmit Line Build Out (LBO). The Line Build Out (LBO) feature allows the transmitter output to be degraded to approximate the defined signal at the cross–connect point (STSX–n). When LBO is not enabled, the transmitter output is unfiltered (STS–n), but will meet the Bellcore 253 specifications at the downstream cross–connect point. When LBO is enabled, the output signal conforms to Bellcore 253 specifications without any further filtering.

Electrical–to–Optical Converter. The Electrical–to–Optical Converter is a self–contained module that converts NRZ ECL differential signals (52 Mb/s, 155 Mb/s, and 622 Mb/s) to optical output.

The Electrical–to–Optical Converter also monitors the laser bias point for end–of–life, excess heat, or low bias conditions. The normal operating range of this voltage is

between 0.010 V and 0.650 V, while end of useful life is indicated by a bias voltage of greater than 0.650 V.

While the A03 CPU processor system controls CTS main function, the A06 Front Panel has its own dedicated processor. The A03 CPU processor system sends instructions to and receives information from the Front Panel Processor on the A06 Front Panel board. The Front Panel Processor monitors the settings of the front–panel switches and knob (potentiometer). Any changes in their settings are reported to the processor system. The Front Panel Processor also controls the front–panel LEDs and generates the beeper signal.

A06 Front Panel

Front Panel Processor. The Front Panel Processor system consists of a single–chip microprocessor with built–in RAM, ROM, A/D converter (for digitizing the potentiometer wiper voltages), a programmable timer (for generating the outputs for the beeper), and a serial communications interface (for data transfer to and from the A03 CPU processor).

Front Panel Controls. All of the front panel controls are "soft" controls in that they are not connected directly into the signal path. The analog output levels of the front–panel knobs/potentiometers are converted to digital equivalents. Therefore, associated circuits are not influenced by the physical parameters of the controls (such as capacitance, resistance, and inductance). Buttons that are pressed are interpreted by the main CPU which converts the identification numbers reported by the Front Panel Processor into the logical functions each button represents. This mapping may be dynamic and depends upon the current operational state of the instrument. For instance, the bezel buttons located underneath and to the right of the display have a logical function which corresponds only to the current menu which is displayed.

There is no correlation between the absolute potentiometer voltage and a knob setting in the main CPU. This is due to the fact that only change information is sent from the Front Panel Processor to the main CPU.

NOTE. The *ON/STBY* switch is not read by the Front Panel Processor. The signal passes through the A06 Front Panel board, is processed by the A03 CPU board, and is passed through the A02 Backplane board to the low voltage power supply.

Communication. A Dual Asynchronous Receive/Transmit (DUART) integrated circuit on the A03 CPU board controls and synchronizes data transfers between the main CPU and the Front Panel Processor. Data transfers between the two processors are initiated by one processor putting data into the DUART, which causes an interrupt to the other processor.

When the power is turned on, the main CPU configures the Front Panel Processor, providing specific information about the front panel controls. The Front Panel Processor needs this information to report changes correctly and to generate the proper outputs for the beeper. Once the Front Panel Processor has been configured, the main CPU goes on with other functions.

A08 Clock Generator

The A08 Clock Generator generates the various clock rates needed by the Protocol boards and Tributary options. The primary purpose of the A08 Clock Generator is to provide a timing source for the transmitter. The A08 Clock Generator also generates the user–selectable clock offsets used to simulate the line frequency offset, payload frequency offset, or tributary rate offset. These offsets can also be configured to provide pointer movements (either AU, VT, or TU pointers).

The A08 Clock Generator must select a reference source for the transmit rate. The reference source can be an internal oscillator, the received line clock, or the external BITS or 2 Mb/s clock references, described below. These clock sources are fed through a multiplexer; selection is controlled by CPU interface circuitry on the A08 Clock Generator board. The clock sources then go through a phase–locked loop to generate a 51.84 MHz reference, which goes back to the Protocol Processor as reference for the transmitter.

The reference sources for the A08 Clock Generator follow:

Internal Oscillator. This crystal oscillator is a Stratum 3–level time base used as the internal reference.

Received Line Clock for Loop Timing. This signal can originate from several places. A mux located on the LS Protocol board selects the signal for forwarding to the Clock board. For STM-0 rates, the clock signal is recovered on the Plug-In-Module. For other STM-n rates, the clock is recovered on the HS Protocol board by the “SERI” chip. For PDH rates, the clock is recovered on the Tributary Option board. Presently, this selection is not used. (Recovered loop-timed test is done by selections on the Tributary board. A copy of the recovered clock is sent to the LS Protocol board over the COMBUS for future features using the JAWA option.)

External BITS Reference or External 2 Mb/s Reference. Input is through a rear–panel jack. The input signal goes through a jitter reduction circuit before being fed to the multiplexer.

Any of these reference sources can be offset by means of a synthesizer on the A08 Clock Generator board.

Protocol Processor

Functionally, the A09 Main Protocol board and the A10 High Speed Protocol board can be considered a single unit, the Protocol Processor. The Protocol Processor is responsible for all generation, acquisition and manipulation of the transport overhead (TOH). If no Tributary option is present, the Protocol Processor also controls the generation and acquisition of the path overhead (POH) and payload.

The Tx part of the Protocol Processor takes data (the data is either internally generated or comes from the option boards via the Com Bus), attaches user–specified POH and TOH values, develops the user–specified multiplex structure, and converts this SDH–compatible parallel data stream to serial format. This serial data stream then goes to the Plug–In Interface Module for final line conditioning and transmission.

The Rx part of the Protocol Processor accepts data from the Plug–In Interface Module, verifies the TOH, demultiplexes the SDH stream, verifies the POH of the demultiplexed stream, and delivers this data stream to the option boards. The Protocol Processor can also take the demultiplexed data and verify the content of the payload.

The Protocol Processor also generates the Tx rate clocks needed for the specified Tx rate. The specified Tx rate is developed from the timing clock received from the A08 Clock Generator or the JAWA option. The Protocol Processor also develops the Tx SDH clock needed by any Tributary boards that are installed.

The functional split between the A09 Main Protocol board and the A10 High Speed Protocol board is listed in Tables 3-1 and 3-2.

Figure 3-2 is a block diagram of the Protocol Processor.

Table 3-1: A09 Main Protocol Board Hardware Function Assignments

A09 Main Protocol Board Elements	Description
PTX	POH content, alarms and pointer movements, internally generated payloads
PRX	POH acquisition and alarm status, pointer movement counters, and SPE PRBS error counters
HWT	Hardware Timer, controls error and pointer insertion rates
DCC Control	Data communications channel control (section DCC and line DCC)
Com Bus Interface	Primary internal interface for passing SDH data to the option boards
Processor Interface	Control register and decode logic
FLASH EPROM	Holds the configuration data for the various XILINX FPGAs used on the board; the main CPU can program the FLASH EPROM contents

Table 3-2: A10 High Speed Protocol Board Hardware Function Assignments

A10 High Speed Protocol Board Elements	Description
SETI	For 155 Mb/s and 622 Mb/s only, parallel–to–serial conversion, CMI encoding/decoding, transmit line clock generation for 155 Mb/s and 622 Mb/s
SERI	For 155 Mb/s and 622 Mb/s only, serial–to–parallel conversion and clock recovery
STTX	SDH section DCC and F1 insertion; LOS and LAIS alarms; SDH line DCC insertion; Line FERF alarm; for 52 Mb/s, parallel–to–serial conversion
ITX	TOH, Tx multiplex structure, inactive channel content, and active channel selection
IRX	TOH acquisition and active channel selection
Clock Generator	Generates the Tx rate clocks needed for the specified Tx rate

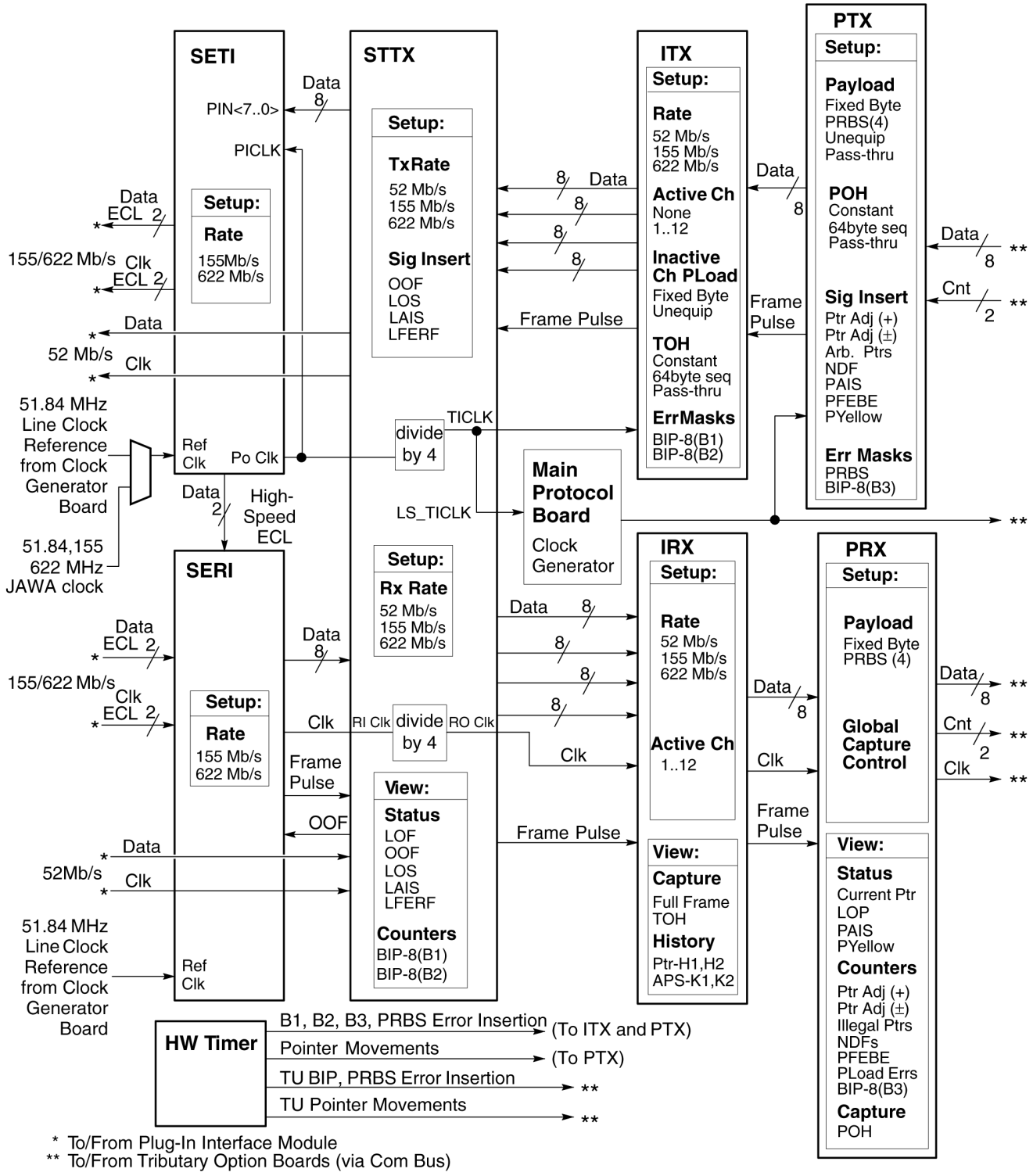


Figure 3-2: Protocol Processor Functional Block Diagram

A25 Low Voltage Power Supply

The low voltage power supply provides the +5.1 V, +15 V, -6.4 V, and -15 V supply voltages to the CTS.

The low voltage power supply is a switching power converter. It supplies power to all instrument circuitry. The low voltage power supply sends power to the A02 Backplane where it is distributed to other boards plugged into the Backplane. Power is also taken directly from the power supply and sent to the Protocol boards (via a cable harness).

The POWER switch controls all power to the instrument including the low voltage power supply. The ON/STBY switch, located on the front panel, also controls all of the power to the instrument except for part of the circuitry in the low voltage power supply.

The monitor is a raster scan cathode–ray tube (CRT) display that has 60 Hz frame and 32 kHz line rates. The CRT display circuitry is similar to that of a television monitor.

A26 Monitor

All information is displayed by the A20 CRT Driver. The driver generates the high voltages necessary to drive the CRT. It also contains the video amplifier, horizontal oscillator, and the vertical and horizontal yoke driver circuitry. The monitor gets its supply voltages from the A25 Low Voltage Power Supply through the A02 Backplane and the A07 Auxiliary Power boards. The monitor receives video signals from the A01 Display board.

The fan provides forced air cooling for the CTS. It connects to +12 V on the A02 Backplane through the A07 Auxiliary Power board.

A14/A16 Tributary Board (Option 38 and 55)

The Tributary board generates test signals and maps and demaps external signals into or out of the payload. The payload interface from the Tributary board to the rest of the CTS is through the Com Bus. The Tributary board is controlled by the A03 CPU via the System Bus.

The COMBUS provides a byte wide STM-1 like data stream with qualifier signals so the SDH payload and POH can be identified. The option allows for more detailed processing and generation of VC-4 payloads. Also, PDH mux/demux capabilities are brought to the CTS850, which were previously unavailable. Customer access to the PDH tributaries is extensive: PDH can be mapped/demapped to/from SDH, generated or monitored internally, or retransmitted while being monitored (passive through mode).

Jitter FIFOs are provided in the PDH transmit path for the possible addition of ‘jittered through mode’. Control of the board is done by the CPU using the AT-bus interface. Figure 3-3 is a block diagram of the A14/A16 Tributary Board.

The Tributary board makes connections to Option 14 (JAWA) and internal buses: a processor bus for module control/status and a proprietary communication bus for SDH mapping and demapping.

A PDH input (Receiver input) signal is directed to the appropriate amplifier circuit using a series of relays. One amplifier handles E1, E2, E3, and DS3 while a separate amplifier handles E4. E4 is handled separately because of the bandwidth and voltage levels involved for that rate.

These options allow for three Rx level selections for Unbalanced inputs and four for Balanced inputs. The E4 Rx (unbalanced only) uses custom automatic cable equalizers that are dependent on the peak-to-peak voltage level applied to its input. Consequently, fixed gain amplifiers are cascaded for the two monitor point selections. The output of each amplifier is input to a custom equalizer. The outputs of the three equalizers are then selected directly by the user for use by other circuitry. The E1, E2, E3, DS3 Rx (unbalanced and E1 Rx balanced) use a common amplifier circuit. A portion of the amplifier is automatic (AGC) and another portion has a fixed gain. The single output of the amplifier is then used by other circuitry.

Clock and Data Recovery is separate for each PDH rate. E4 is always CMI decoded and E1, E2, E3 can be either AMI or HDB3. DS3 can be either B3ZS or HDB3. Decoder outputs are NRZ data and clock, which are used by other circuits.

Demappers are provided to extract a VC-4 payload from SDH as a C-4 (E4), C-3 (E3 or DS3), or C-12 (E1). Each payload is passed through a Desynchronizer circuit to reduce jitter and obtain a smooth clock.

Received PDH signals or Demapped signals can be demultiplexed into sub-rates. Sub-rates can be monitored for frame or PRBS errors and also directed to the PDH Transmitter output.

Demultiplexing to 64Kb/s channel can be dropped to a chassis mounted speaker. DS3 has no Mux/Demux capabilities.

Low rate PDH Receive or Demapped signals can be directed to the PDH Multiplexer (Generator) for insertion into higher rate PDH signals. The multiplexer output can be directed to the VC-4 mapper or to the PDH Transmitter output.

Mappers are provided for E1, E3, and E4 for:

- E1 > C12 > VC12 > TU12 >VC4
- E3 > C3 > VC3 > VC4
- DS3 > C3 > VC3 > VC4
- E4 > C4 > VC4

Phase-Locked Loops create transmit clocks for internally generated PDH signals. The reference for the PLLs is a customer supplied clock (BITS, 2.048MHz, 2.048Mb/s) or an internal precision oscillator.

Generator (Tx) Clock Multiplexer selects timing source for the internal PDH generator/mux. The generator clock can be: internal PLL, internal Jittered Clock, Recovered Line clock, or Demapped/desynchronized clock.

Line (Tx) Clock Multiplexer selects timing source for the PDH line output. Typically, the selection is identical to the Generator but the possibility of applying jitter to a

Recovered Line clock is provided by this mux. FIFOs are between the Generator MUX and the Line drivers to support this feature.

PDH Line Drivers for each rate are directed to the BNC connection or Balanced (E1 only) using relays.

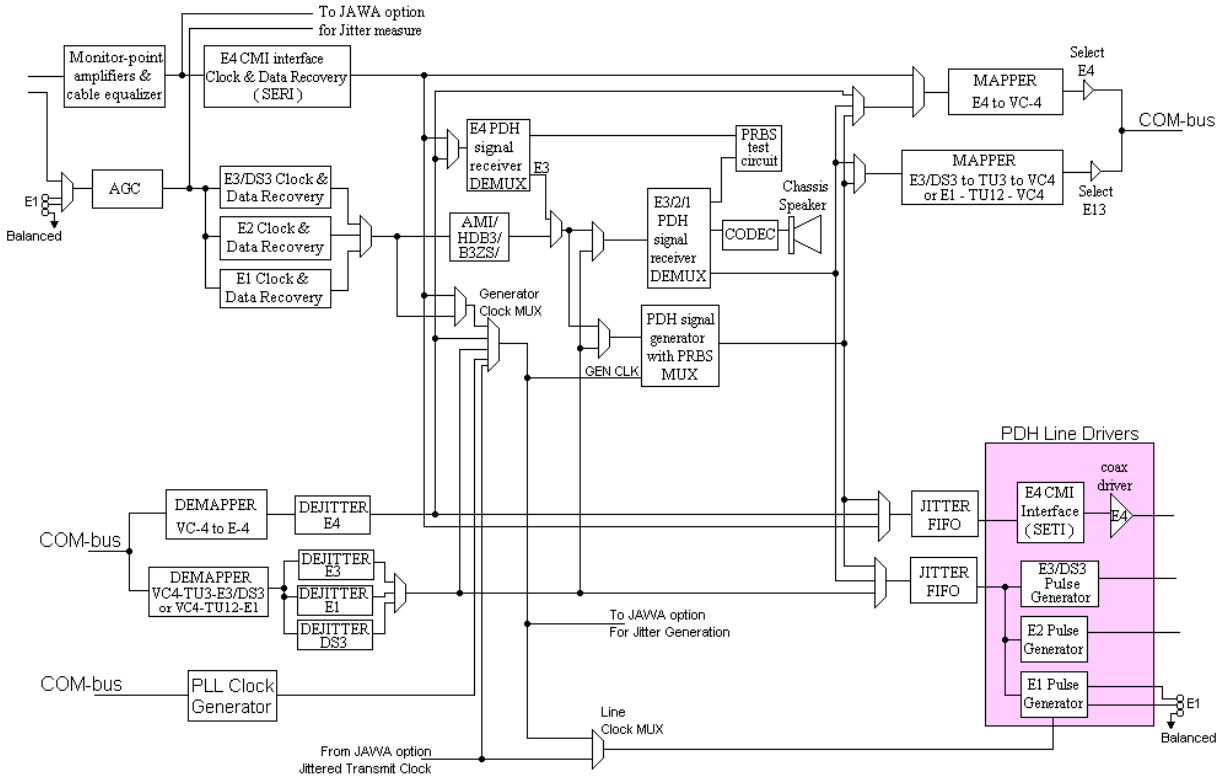


Figure 3-3: Tributary Board Functional Block Diagram

A14 JAWA and JAWG Board Pair (Option14)

Option 14 includes the A14 JAWG (jitter and wander generator) and A12 JAWA (jitter and wander analyzer) circuitry.

JAWG board

The JAWG board generates a clock signal that is modulated by wander or jitter at a programmed frequency and amplitude. The CTS can use the jittered clock (in place of a stable clock) to set the timing of the transmit outputs for each of the data rates. The jittered clock is also available as an output at the rear panel. Figure 3-4 shows a block diagram of the JAWG circuitry.

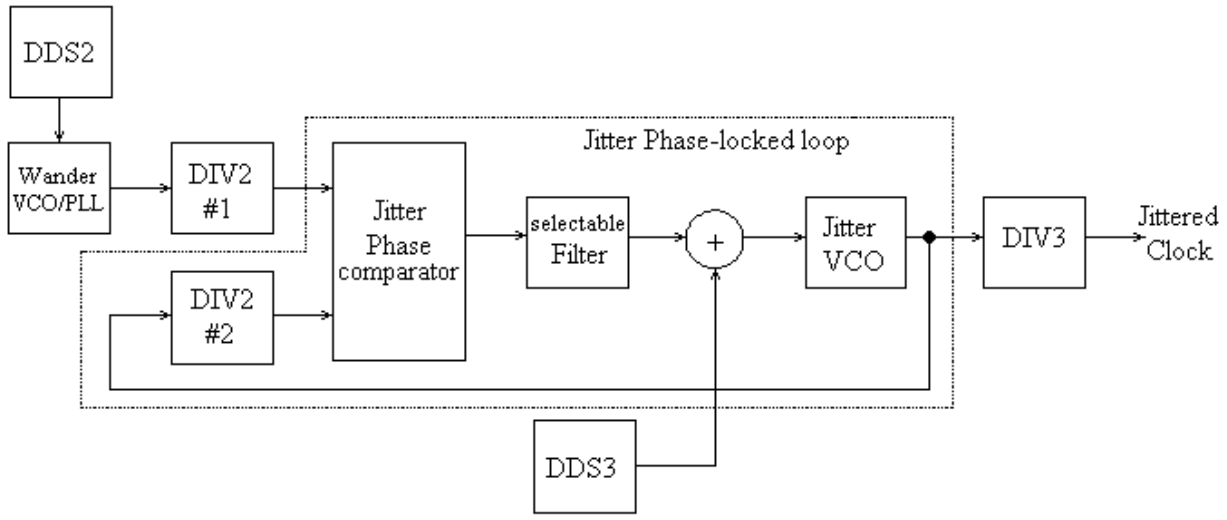


Figure 3-4: JAWG Block Diagram

DDS2. Clock timing is based on direct digital synthesis (DDS) at a nominal 4.86 MHz, which is then multiplied up to the clock frequency by the voltage controlled oscillator VCO in phase-locked loop.

Wander VCO/PLL. This block is an oscillator that sets the nominal clock frequency and generates low frequency modulation for the JAWG.

Wander and jitter with modulation frequencies below 1 KHz is generated directly by reprogramming the DDS1 output frequency in real time.

DIV2 #1 and DIV2 #2. There are two matching frequency dividers labeled DIV2 that set the jitter generation amplitude range. Frequency dividers are required prior to the phase comparator to generate jitter amplitudes greater than one unit interval.

DDS3. The DDS3 block generates the jitter modulation frequency using direct digital synthesis. Its output amplitude, which is programmable, determines the jitter modulation amplitude of the jittered clock for modulation frequencies of 1 KHz and above.

Jitter Phase–Locked Loop. The phase comparator begins the phase–locked loop that generates the jittered clock. The filter, summer, and VCO complete the phase–locked loop.

When generating jitter with modulation frequencies above 1 KHz, the Wander PLL/VCO block supplies the nominal clock frequency. The summer adds the jitter frequency, which is above the loop bandwidth, to modulate the clock frequency.

DIV3. Frequency divider DIV3 divides the phase–locked loop output frequency down to the clock rate required by the CTS. The divider ratio is determined by the transmit rate setting.

JAWA board

The JAWA (jitter and wander analyzer) board measures peak–to–peak or RMS jitter from the received line signal or from a rear–panel clock input. Figure 3-5 shows a block diagram of the JAWA circuitry.

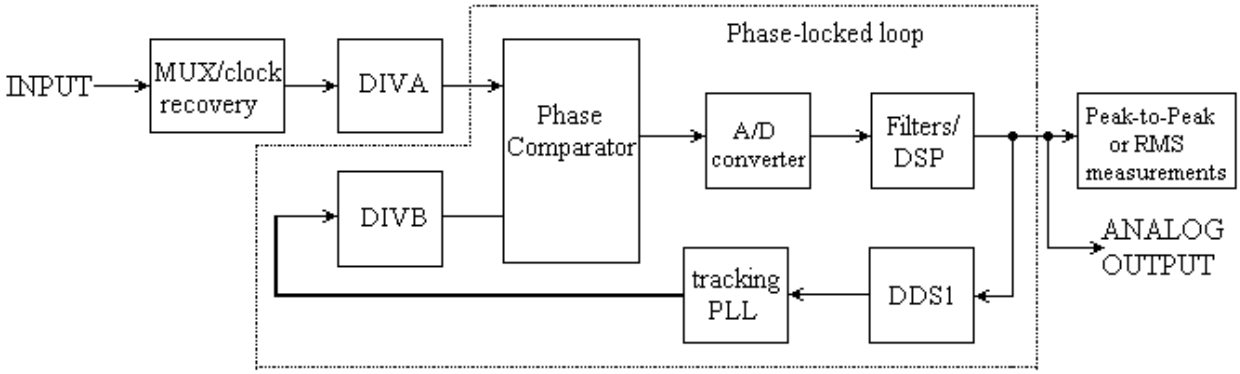


Figure 3-5: JAWA Block Diagram

MUX/Clock Recovery. The multiplexer and clock recovery block selects the source to be measured and, if necessary, recovers a clock from it.

DIVA. Frequency divider DIVA divides the frequency of the source. A frequency divider is required prior to the phase comparator in order to measure jitter amplitudes greater than one unit interval.

Phase–Locked Loop (PLL). The phase–locked loop(PLL) tracks the frequency of the divided input source. The loop consists of a phase comparator, an A/D converter, a digital filter and digital signal processing (DSP) block, a DDS1 block, a tracking PLL, and another frequency divider, DIVB.

The digital filters and DSP block set programmable cutoff frequencies for the jitter measurement filters. The DSP function also maintains lock in the loop by controlling the output frequency of the DDS1 block.

The DDS1 is followed by a tracking phase–locked loop. A reference frequency is generated using direct digital synthesis (DDS) under control of the DSP function. The VCO is part of a phase–locked loop that multiplies the DDS output frequency by a factor of 128.

Frequency divider DIVB divides the VCO output frequency so that both inputs to the phase comparator are at the same nominal frequency.

Peak-to–Peak or RMS Measurement. The digital output from the DSP function contains the data necessary to calculate peak–to–peak or RMS jitter and wander in the input signal. This data is passed to the CPU to report data to the user.

Analog Output. An analog signal, proportional to the demodulated jitter, is available on the rear panel. This signal will normally show sine waves when test jitter signals are being received.

Performance Verification

The performance verification procedures in this section are for the CTS850 SDH/PDH Test Set. You may only need to perform a few of these procedures, depending on what you want to accomplish. Refer to Table 4-1 to determine which procedures you need to do.

Table 4-1: CTS Performance Verification Guide

If What You Want to Accomplish is	Perform These Procedures	Approximate Time to Complete
Quick test of CTS	Self Test	Ten minutes
Thorough test of the functionality	Functional Tests	Twenty minutes
Verification of warranted specifications	Functional Tests Physical Layer Tests	Twenty minutes Two hours
Verification of Option 38 - PDH Tributaries	Tributaries	One hour
Verification of Option 14 - Jitter	Jitter Tests	Three hours and twenty minutes
Verification of Option 55 – 45 MB/s support		

General Information and Conventions

Please read the following general information and conventions, which apply throughout this section:

⇒ Each test procedure begins with a table, similar to the one below, that provides information you need to know before starting the test.

Equipment Required	Tektronix TDS784C (see item 30 in Table 4-2) SMA male–to–BNC female adapter (item 20)
Prerequisites	All previous Physical Layer Tests
Time Required	Approximately ten minutes

The item numbers after each piece of equipment refer to line numbers in Table 4-2, *Required Test Equipment*. The time estimates assume all the necessary equipment has been gathered, and that the equipment is warmed up and is ready to use.

⇒ This manual presents setup instructions for the CTS in tables. Perform the steps reading from left to right in the table (see example below).

Press Menu Button	**Select Menu Page**	**Highlight Parameter**	**Select Choice**
Begin here with Step 1	Step 2	Step 3	Step 4
		Step 5	Step 6
		Step 7	Step 8, setup is complete

Menu buttons are located on the instrument front panel (see Figure 4-1). Select menu pages with the buttons below the display. Use the knob to highlight a parameter; then use the buttons at the right side to select a choice. Many setups require several iterations of highlighting parameters and selecting choices. Some setups may require more than one menu button or menu page selection as well.

NOTE: *For more instructions on the general use of the CTS850 and on navigating through the CTS850 front panel menus, refer to the CTS850 User Manual (Part #070-9988-xx)*

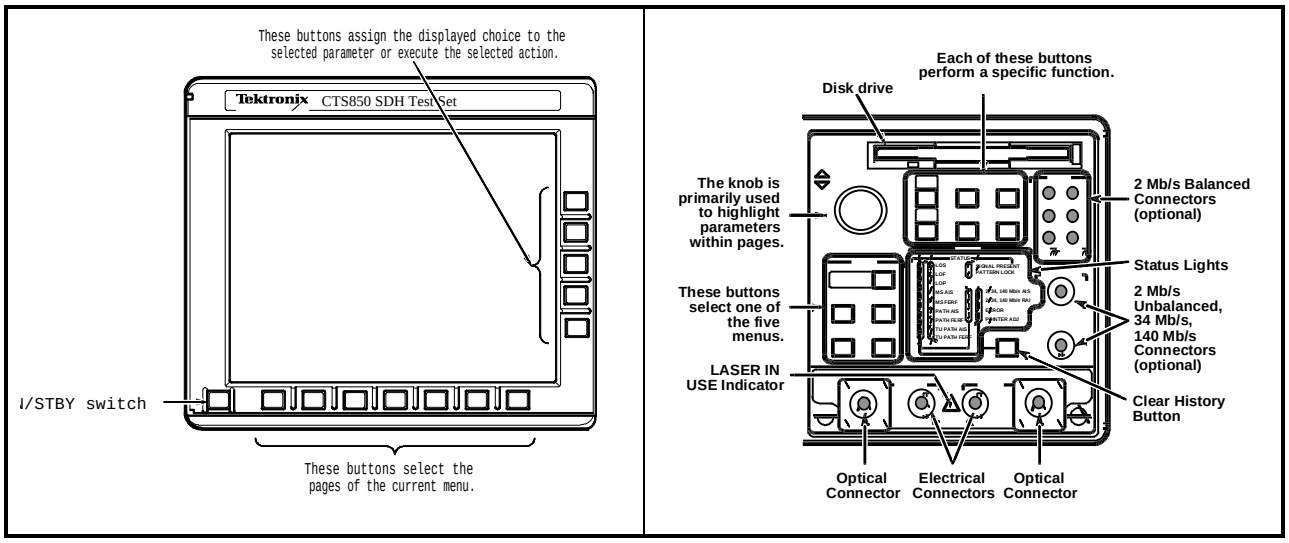


Figure 4-1: Location of Front–Panel Controls

Equipment Required

The *Physical Layer Tests* use traceable signal sources and measurement instruments to check performance. Table 4-2 lists the required equipment. However, some specific items may not be required depending on the exact configuration of your CTS.

You can obtain an accuracy ratio of 4:1 or better by using the recommended equipment listed in the *Example* column of Table 4-2. If your test equipment does not meet the minimum requirements listed in the table, your test results may be invalid.

Table 4-2. Required Test Equipment

Item #/ Description		Minimum Requirements	Example	Purpose
1	Universal Counter/Timer	160 MHz frequency measurement capability; frequency ratio B/A capability; 0.25 ppm time base accuracy; 9 digits; averaging to 10^8	Tektronix DC 5010 Digital Counter/Timer with TM 5000 mainframe (if available), or an HP53131A Universal Counter with Option 001	Checking transmit clock accuracy
2	Signal Generator	750 kHz to 630 MHz frequency range; ≤10Hz resolution below 30 MHz; ≤50Hz resolution from 300 MHz to 320 MHz; ≤100Hz resolution from 600 MHz to 630 Mhz; ≤1 ppm frequency error; +13 dBm sine wave output into 50 Ohm	Rohde & Schwarz Signal Generator SME 02	Checking clock inputs
3	Digital Scope	Tektronix TDS784C Digital Scope with: Opt 2C (masks) and Opt 4C (P6703B O/E converter)	If TDS784C is unavailable, the TDS784D with the appropriate options may be used in place of it.	Checking transmit signal shape, mask testing, and analog output testing.
4	2/8/34/140 Mb/s Signal Source	Provides 2 Mb/s signal	Tektronix CTS 850 Test Set (in addition to the CTS–under–test)	Checking 2 Mb/s Reference Input and Add/Drop/Test
5	Optical Attenuator	Compatible with single mode fiber; attenuation range from 0 dB to 50 dB for λ = 1310 nm, 1550 nm	FVA-60A Optical Attenuator, EXIO Electro-optical engineering	Check receiver sensitivity
6	Optical Power Meter		Tektronix TFC200 with option 21 (FC conn)	Check transmit signal power and shape
7	Spectrum Analyzer	Frequency range 2 Mhz to 1 Ghz	Advantest R3271A, opt.14; N-BNC adapter 103-0045-00	Check jitter generation on clock outputs
8	Optical Fiber Cable 2M (two required)	Single mode fiber; FC/PC connector on one end; compatible with connector option on other end	FC/PC–to–FC/PC, Tektronix part number 174–1387–00	Interconnect optical signals
9	10 dB Optical Attenuator	10 dB attenuation at λ = 1550 nm, with connectors compatible with item 12 and connector option.	Tektronix part number 119–1387–00	Provide optical attenuation at 1550 nm
10	100 ft (31 m) length of 75 Ohm Reference Cable	BNC connectors on each end	AT&T 728B reference cable	Check receiver sensitivity
11	225 ft (68.6 m) length of 75 Ohm Reference Cable, (two required)	BNC connectors on each end	AT&T 728B reference cable	Check receiver sensitivity
12	75 Ohm Coaxial Cable, (three required)	75 Ohm impedance; 2M length, BNC connectors	Tektronix part number 012–1338–00	Interconnect electrical signals

Table 4-2. Required Test Equipment (continued)

Item #/ Description		Minimum Requirements	Example	Purpose
13	Adapter, BNC Female–to–BNC Female, (two required)	50 Ohm impedance; BNC female connectors	Tektronix part number 103–0028–00	Splicing long cable lengths
14	Adapter, Type N Male–to–BNC Female	50 Ohm impedance	Tektronix part number 103–0045–00	Interconnect electrical signals
15	50 Ohm SMB–to–BNC Coaxial Cable	50 Ohm impedance; SMB female connector to BNC male connector	Tektronix P6041	Clock accuracy verification.
16	120 Ohm Cable, DIN41628L Male–to–DIN41628L Male (two required)	Three–conductor cable; DIN41628L (Siemens) jack on both ends	Tektronix part number 012–1469–00	Interconnect electrical signals
17	10X (20dB) Attenuator	75 Ohm impedance; 10X (20 dB) attenuation; BNC connectors	Mini–Circuits part number CAT–20–75	Interconnect electrical signals
18	2X (6dB) Attenuator	75 Ohm impedance; 2X (6 dB) attenuation; BNC connectors	Mini–Circuits part number CAT–6–75	Interconnect electrical signals
19	3dB Attenuator	75 Ohm impedance; 3dB attenuation; BNC connectors	Mini-Circuits part number CAT-3-75	Interconnect electrical signals
20	10dB Attenuator	75 Ohm impedance; 10dB attenuation; BNC connectors	Mini-Circuits part number CAT-10-75	Interconnect electrical signals
21	50 ohm terminator	50 Ω impedance, BNC connectors	Tektronix part number 011-0019-01	Interconnect electrical signals
22	Adapter, BNC male to BNC male	50 Ω impedance, BNC male connectors	Tektronix part number 103-0029-00	Interconnect electrical signals
23	106 ft (33m) length of 75 Ω reference cable	BNC connectors on each end	AT&T 728B reference cable	Check cable equalization
24	Optical Filter (STM0)		Tektronix FS52	Optical mask testing
25	Optical Filter (STM1)		Tektronix FS156	Optical mask testing
26	Optical Filter (STM4)		Tektronix FS622	Optical mask testing
27	Adapter probe (120 Ω)	Differential to 50 ohms	Tektronix AFTDS probe	120 ohm mask
28	Adapter probe (75 Ω)	75/50 ohm adapter probe	Tektronix AMT75	75 ohm mask
29	Feedthru terminator	50 ohms feedthru	Tektronix part number 011-0049-01	Interconnect electrical signals
30	Tributary Signal Converter/Analyzer	Convert impedance of 120 Ω 2Mb/s tributaries to 50 Ω and attenuate by 5X	Tektronix part number 067-0250-01	Interconnect electrical signals
31	50Ω BNC coaxial cable	50Ω impedance; BNC male connectors	Tektronix part number 012-0057-01	Interconnect electrical signals
32	Adapter, BNC-female to BNC-male	75Ω female BNC to 50Ω male BNC	Mini-Circuits part number BMP-5075R	Interconnect electrical signals

Test Record

Photocopy Table 4-3, found on the next pages, and use it to record the performance verification results for your instrument.

Table 4-3: CTS 850 (SDH/PDH) Test Record

CTS 850 Serial Number:	Temperature and Relative Humidity:
Plug–In Interface Module Type:	Verification Performed by:
Plug–In Interface Module Serial Number:	Date of Verification:

CTS 850 Functional Tests

Test		**Passed**	**Failed**
System Self Test with External Loop–Back			
Generated Failures	None		
	LOS		
Pointer Movements	Continuous		

CTS 850 Physical Layer Tests

Transmit Output Checks		**Minimum**	**Measured Value**	**Maximum**
Electrical Signal Level at Transmit Output	STM-0E 0dB	900 mV_{pk}		1.1 V_{pk}
	STM–1E 0dB	900 mV_{pp}		1.1 V_{pp}

		Measurement Type	**Passed**	**Failed**
Electrical Output Pulse Shape	STM–0E -6dB	Mask		
	STM-0E 0dB	Mask		
	STM–1E -6dB	Mask		
	STM-1E 0dB	Pulse Template		
Optical Output Pulse Shape	STM-0			
	STM–1			
	STM–4			

Optical Output Power	**Minimum**	**Measured Value**	**Maximum**
Option 03, 04	-12dB	- - - - -	-7 dB
STM-0			
STM-1			
STM-4			
Option 05	-3 dBm	- - - - -	+2 dBm
STM-0			
STM-1			
STM-4			

Table 4-3: CTS 850 (SDH/PDH) Test Record (continued)

Receive Input Checks		**Passed**	**Failed**
Electrical Input Sensitivity	STM-0E 0dB		
	STM–0E -6dB		
	STM–0E -12dB		
	STM–0E Monitor		
	STM–1E 0dB		
	STM-1E -6dB		
	STM-1E -12dB		
	STM-1E Monitor		
Optical Input Sensitivity	STM-0		
	STM–1		
	STM-4		

Transmit Clock Checks		**Minimum**	**Measured Value**	**Maximum**
Internal Clock Accuracy		51,839,762 Hz		51,840,238 Hz
Transmit Line Frequency Offset	Positive	51,844,946 Hz		51,845,422 Hz
	Negative	51,834,578 Hz		51,835,054 Hz
2 Mb/s Reference Input		0.019752		0.019754

Table 4-3: CTS 850 (SDH/PDH) Test Record (continued)

Tributary Checks (Option 38)

Electrical signal level at Transmit Output	Minimum	Measured Value	Maximum
2 Mb/s Balanced	2.700 Vpk		3.300 Vpk
2 Mb/s Unbalanced	2.133 Vpk		2.607 Vpk
8 Mb/s Unbalanced	2.133 Vpk		2.603 Vpk
34 Mb/s Unbalanced	0.900 Vpk		1.100 Vpk
140 Mb/s Unbalanced ALL ONES	0.900 Vpp		1.100 Vpp
140 Mb/s Unbalanced ALL ZEROS	0.900 Vpp		1.100 Vpp
45 Mb/s Unbalanced (*Option 55 only*)			
0 dB (+450 ft cable)	0.36 Vpk		0.85 Vpk
-6 dB (+ 0 ft cable)	0.36 Vpk		0.85 Vpk

Transmit Pulse Mask	Passed	Failed
2 Mb/s Balanced		
2 Mb/s Unbalanced		
8 Mb/s Unbalanced		
34 Mb/s Unbalanced		
140 Mb/s Unbalanced		
45 Mb/s Unbalanced (Option 55 only)		
0 dB (+450 ft cable)		
-6 dB (+0 ft cable)		

Receiver Sensitivity	Passed	Failed
2 Mb/s Balanced Normal		
2 Mb/s Balanced 20 dB Mon		
2 Mb/s Balanced 30 dB Mon		
2 Mb/s Balanced Bridge		
2 Mb/s Unbalanced Normal		
2 Mb/s Unbalanced 20 dB Mon		
2 Mb/s Unbalanced 30 dB Mon		
8 Mb/s Unbalanced Normal		
8 Mb/s Unbalanced 20 dB Mon		
8 Mb/s Unbalanced 30 dB Mon		
34 Mb/s Unbalanced Normal		
34 Mb/s Unbalanced 20 dB Mon		
34 Mb/s Unbalanced 30 dB Mon		
140 Mb/s Unbalanced Normal		
140 Mb/s Unbalanced 20 dB Mon		
140 Mb/s Unbalanced 30 dB Mon		
45 Mb/s Unbalanced (Option 55 only) Normal		

20 dB Mon		

Table 4-3: CTS 850 (SDH/PDH) Test Record (continued)

Low–Frequency Jitter Tests (Option 14 only)			**Jitter Measurement Tests**		
Jitter Frequency	**Jitter Amplitude**	**Transmit Rate**	**Minimum**	**Measured Value**	**Maximum**
15 Hz	200 UI Amplitude	2 Mb/s (Unbalanced)	189.29 UI		209.82 UI
		34 Mb/s	189.29 UI		209.82 UI
		140 Mb/s	189.29 UI		209.82 UI
		STM–0E	189.29 UI		209.82 UI
		STM–1E	189.29 UI		209.82 UI
		STM–4	188.79 UI		210.32 UI
		45Mb/s *(Option 55 only)*	189.29 UI		209.82 UI
150 Hz Jitter Frequency	16 UI Amplitude	2 Mb/s (Unbalanced)	14.82 UI		16.61 UI
		34 Mb/s	14.82 UI		16.61 UI
		140 Mb/s	14.82 UI		16.61 UI
		STM–0E	14.82 UI		16.61 UI
		STM–1E	14.82 UI		16.61 UI
		STM–4	14.67 UI		16.76 UI
		45Mb/s *(Option 55 only)*	14.82 UI		16.61 UI

Table 4-3: CTS 850 (SDH/PDH) Test Record (continued)

High–Amplitude Jitter Tests (Option 14 only)		Jitter Generation Tests			Jitter Measurement Tests		
Transmit/Clock Rate	**Jitter Frequency**	**Min.**	**Measured Value**	**Max.**	**Min.**	**Measured Value**	**Max.**
2 Mb/s (Unbalanced)	2.5 KHz	1.64 UI		1.88 UI	1.637 UI		1.883 UI
2 Mb/s (Unbalanced)	1.8 KHz	8.28 UI		9.22 UI	8.27 UI		9.22 UI
2 Mb/s (Unbalanced)	6.4 KHz	2.58 UI		2.92 UI	2.577 UI		2.922 UI
2 Mb/s (Unbalanced)	100 KHz	0.70 UI		0.83 UI	—	*(not tested)*	—
34 Mb/s	2.5 KHz	1.64 UI		1.88 UI	1.635 UI		1.882 UI
34 Mb/s	8 KHz	8.28 UI		9.22 UI	8.27 UI		9.22 UI
34 Mb/s	26 KHz	2.58 UI		2.92 UI	2.577 UI		2.922 UI
34 Mb/s	100 KHz	0.70 UI		0.83 UI	0.692 UI		0.838 UI
34 Mb/s	800 KHz	0.70 UI		0.83 UI	—	*(not tested)*	—
140 Mb/s	2.5 KHz	1.63 UI		1.89 UI	1.631 UI		1.878 UI
140 Mb/s	10 KHz	8.27 UI		9.23 UI	8.27 UI		9.22 UI
140 Mb/s	50 KHz	2.57 UI		2.93 UI	2.577 UI		2.922 UI
140 Mb/s	3.5 MHz	0.69 UI		0.84 UI	—	*(not tested)*	—
STM–0E	2.5 KHz	1.64 UI		1.88 UI	1.635 UI		1.882 UI
STM–0E	5 KHz	1.64 UI		1.88 UI	1.637 UI		1.883 UI
STM–0E	10 KHz	8.28 UI		9.22 UI	8.27 UI		9.22 UI
STM–0E	26 KHz	2.58 UI		2.92 UI	2.577 UI		2.922 UI
STM–0E	400 KHz	0.70 UI		0.83 UI	—	*(not tested)*	—
STM–1E	5 KHz	1.63 UI		1.89 UI	1.627 UI		1.876 UI
STM–1E	10 KHz	8.28 UI		9.22 UI	8.27 UI		9.21 UI
STM–1E	26 KHz	5.42 UI		6.08 UI	5.426 UI		6.072 UI
STM–1E	1.3 MHz	0.69 UI		0.84 UI	—	*(not tested)*	—

Table 4-3: CTS 850 (SDH/PDH) Test Record (continued)

High–Amplitude Jitter Tests (Option 14 only)		**Jitter Generation Tests**			**Jitter Measurement Tests**		
Transmit/Clock Rate	**Jitter Frequency**	**Min.**	**Measured Value**	**Max.**	**Min.**	**Measured Value**	**Max.**
STM–4	10 KHz *(first test)*	1.56 UI		1.96 UI	1.592 UI		1.911 UI
STM–4	10 KHz *(second test)*	8.27 UI		9.23 UI	8.19 UI		9.22 UI
STM–4	68 KHz	5.35 UI		6.15 UI	5.392 UI		6.107 UI
STM–4	600 KHz	0.62 UI		0.91 UI	0.611 UI		0.802 UI
45Mb/s *(Option 55 only)*	2.3 KHz	1.63 UI		1.89 UI	1.637 UI		1.883 UI
45Mb/s *(Option 55 only)*	10 KHz	8.27 UI		9.23 UI	8.27 UI		9.22 UI
45Mb/s *(Option 55 only)*	26 KHz	2.57 UI		2.93 UI	2.577 UI		2.922 UI
45Mb/s *(Option 55 only)*	60 KHz	0.69 UI		0.84 UI	0.692 UI		0.838 UI

Table 4-3: CTS 850 (SDH/PDH) Test Record (continued)

Low–Amplitude Jitter Tests (Option 14 only)		**Jitter Generation Tests**			**Jitter Measurement Tests**		
Transmit Rate	**Jitter Frequency**	**Min.**	**Calculated Value = J**	**Max.**	**Min.**	**Measured Value**	**Max.**
2 Mb/s (Unbalanced)	50 KHz	0.255 UI		0.345 UI	J - 0.061 UI		J + 0.049 UI
2 Mb/s (Unbalanced)	100 KHz	0.445 UI		0.555 UI	J - 0.151 UI		J + 0.029 UI
34 Mb/s	800 KHz	0.445 UI		0.555 UI	J - 0.207 UI		J + 0.077 UI
140 Mb/s	400 KHz	0.445 UI		0.555 UI	J - 0.062 UI		J + 0.068 UI
140 Mb/s	3.5 MHz	0.445 UI		0.555 UI	J - 0.207 UI		J + 0.077 UI
STM–0E	400 KHz	0.445 UI		0.555 UI	J - 0.207 UI		J + 0.077 UI
STM–1E	650 KHz	0.445 UI		0.555 UI	J - 0.067 UI		J + 0.063 UI
STM–1E	1.3 MHz	0.350 UI		0.450 UI	J - 0.207 UI		J + 0.077 UI
STM–4	3 MHz	0.225 UI		0.375 UI	J - 0.101 UI		J + 0.079 UI
45Mb/s *(Option 55 only)*	400 KHz	0.435 UI		0.565 UI	J - 0.207 UI		J + 0.077 UI

Self Test with Internal Loopback

This procedure uses internal routines to verify that the CTS 850 SDH/PDH Test Set passes its internal self-tests.

Equipment Required	No test equipment or connections are required
Prerequisites	Power up the CTS and allow a twenty minute warm–up period before running self test
Time Required	Approximately ten minutes (after warm–up time)

Running Self Test

Set up and execute the self-test with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
UTILITY	SELF TEST	Self Test Group	Sys: Internal
		Self Test Control	Run

When the self-test completes, the message PASSED appears in the display. If you see the message FAILED, repeat the self-test. If the problem persists, contact your local Tektronix field office or representative for assistance.

There are advantages and disadvantages of this self-test. One advantage is you do not have to disconnect the CTS from your application. One disadvantage is the electrical and optical I/O circuitry is not verified by the test. If the self-test passes and you are still experiencing difficulty, perform *System Self Test with External Loopback* to test the electrical I/O circuitry.

Functional Tests

The purpose of functional tests is to verify the functional specifications of the CTS850. Most functional tests rely on the front panel status lights, shown in Figure 4-2, to indicate the results of the test.

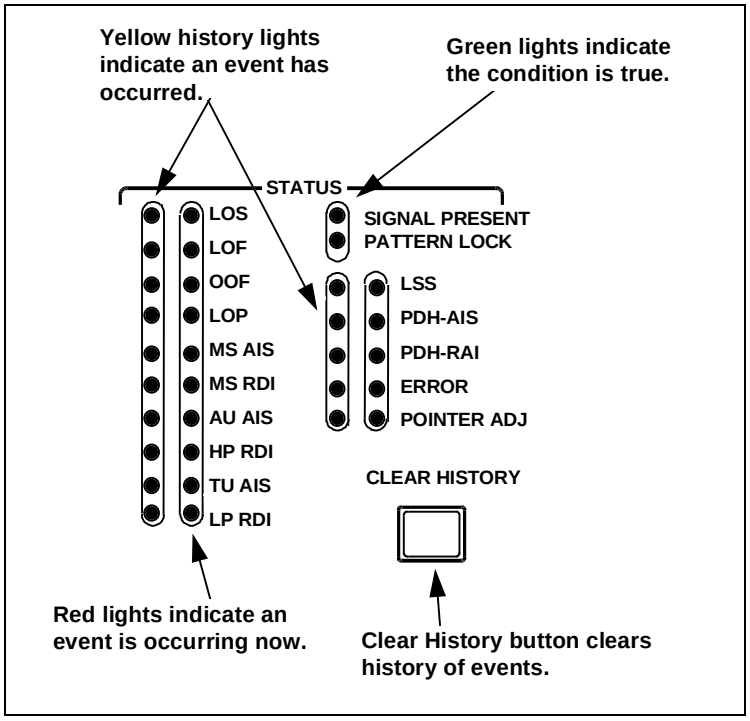


Figure 4-2: Typical Front–Panel Status Lights

Loopback Connection

Each functional test requires an external loopback connection from the TRANSMIT output to the RECEIVE input. For the electrical loopback, you can use the 75 Ohm BNC coaxial cable provided as a standard accessory to the CTS. If one of the Electrical/Optical Plug–In Interface Modules is installed in your CTS, you also need a short optical cable that is compatible with the optical connectors on your instrument. If your CTS has Option 05, connect a 10 dB optical attenuator (included with Option 05) in series with the cable to prevent saturation of the receiver input. Optical cables are not included as standard accessories to the CTS.

If the CTS fails any of these tests, it has failed the performance verification. Double check the electrical and optical connections and repeat any failed test. If the failure persists, contact your local Tektronix field office or representative for assistance.

How to Proceed

You may perform the functional tests in any order. Each test is independent and does not depend on the setup from the previous test.

System Self Test with External Loopback

This test runs the self-test including coverage of the transmitter and receiver I/O circuitry.

Equipment Required	75 Ohm BNC coaxial cable (item 12) for electrical loop–back, one required (two required if Option 38 is installed) Optical loop–back cable (item 8) if Electrical/Optical Plug–In Interface Module is installed 10 dB optical attenuator (item 9) if Option 05 is installed. If Option 38 is installed, 120 Ohm DIN41628L cable (item 16) for electrical loop–back
Prerequisites	CTS warmed–up at least twenty minutes
Time Required	Approximately ten minutes

1. Attach electrical and optical loop–back cables from the TRANSMIT 52/155 Mb/s outputs to the 52/155 Mb/s RECEIVE inputs (include optical attenuator if Option 05).
2. Attach the electrical loop–back cables from the 2/8/34/140 Mb/s OUT outputs to the 2/8/34/140 Mb/s IN inputs.
3. Set up and execute the system self test with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
UTILITY	SELF TEST	Self Test Group	Sys Ext
		Self Test Control	Run

4. After several minutes, read the diagnostic result on the display when the test has completed. The result should read as PASSED.

LOS Generation

This test checks that the CTS detects the LOS failure correctly.

Equipment Required	75 Ohm BNC coaxial cable (item 12) for electrical loop–back
Prerequisites	CTS warmed–up at least twenty minutes
Time Required	Approximately five minutes

1. Attach the 75 Ohm coaxial cable (electrical) from the 52/155 Mb/s TRANSMIT output to the 52/155 Mb/s RECEIVE input.
2. Perform the initial setup of the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Transmit Rate	STM–1E
		Tx/Rx Settings	Coupled

3. Verify that the SIGNAL PRESENT and PATTERN LOCK lights are on.
4. Press the **CLEAR HISTORY** button. After a moment, verify that no red or yellow history lights are on.
5. Remove one end of the 75-ohm coaxial cable from the Transmit Output to the Receive Input.
6. Verify that the red and yellow LEDs for LOS are on.
7. Replace the 75-ohm coaxial cable from the Transmit Output to the Receive Input.
8. Verify that the SIGNAL PRESENT and PATTERN LOCK lights are on.
9. Press the **CLEAR HISTORY** button. After a moment, verify that no red or yellow history lights are on.

10. Perform the initial setup of the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Transmit Rate	STM–0E
		Tx/Rx Settings	Coupled

11. Verify that the SIGNAL PRESENT and PATTERN LOCK lights are on.

12. Press the **CLEAR HISTORY** button. After a moment, verify that no red or yellow history lights are on.

13. Remove one end of the 75-ohm coaxial cable from the Transmit Output to the Receive Input.

14. Verify that the red and yellow LEDs for LOS are on.

15. Replace the 75-ohm coaxial cable from the Transmit Output to the Receive Input.

16. Verify that the SIGNAL PRESENT and PATTERN LOCK lights are on.

17. Press the **CLEAR HISTORY** button. After a moment, verify that no red or yellow history lights are on.

Pointer Movement

This test checks that the CTS generates and measures pointer movement correctly.

Equipment Required	75 Ohm BNC coaxial cable (item 12) for electrical loop–back
Prerequisites	CTS warmed–up at least twenty minutes
Time Required	Approximately five minutes

1. Attach the 75 Ohm coaxial cable (electrical) from the TRANSMIT output to the RECEIVE input.
2. To verify Continuous Pointer Movements, set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Transmit Rate	STM–1E
		Tx/Rx Settings	Coupled
TRANSMIT	POINTERS & TIMING	Pointer Control	Continuous
		Pointer Rate	Max 2 ms
TEST SETUPS	TEST CONTROL	Test Duration	USER DEFINED

3. Press the **Minutes** button and then rotate the knob to **1 m**.
4. Press the **Seconds** button and then rotate the knob to **40 s**.
5. Press the **Done** button to set the test duration to 1 minute, 40 seconds (100 seconds, total).

6. To monitor pointer movements, change the CTS setup with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
RESULTS	SDH RESULTS	*none*	Pointers

7. Press the **START/STOP** button, and verify that the START/STOP light is on.

8. Wait 100 seconds for the test to complete. When the START/STOP light turns off, verify that the Positive Justification and Negative Justification counts meet both of the following conditions:

$$24000 \leq \textit{Positive Justifications} \leq 26000$$

$$\textit{Negative Justifications} = \textit{Positive Justifications} \pm 1$$

9. Change the CTS setup with the following sequence to set the Tx Pointer Control back to 'Single'.

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
Tx	POINTERS AND TIMING	*POINTER CONTROLS*	Single

10. Press the CLEAR HISTORY button. After a moment, verify that there are no yellow ERROR history LEDs lit.

Physical Layer Tests

This section contains a set of procedures that verify that the CTS 850 SDH Test Set meets its physical layer specifications. These procedures check performance of the standard instrument as well as two optional Plug–In Interface Modules, so some steps may not apply to your CTS. The steps that apply only to optional Plug–In Interface Modules are identified in the procedures.

The procedures contain setup instructions for the example equipment listed in Table 4-2, *Required Test Equipment*. You may use equipment other than the recommended examples if it meets the minimum requirements listed. However, if you do, you might need to modify the interconnect diagrams and setup instructions.

Prerequisites for All Physical Layer Tests

The procedures in this section are a valid test of the CTS performance when the following requirements are met:

- All outside covers must be installed on the CTS.
- The CTS has passed all the *Functional Tests*.
- The CTS has warmed up for at least 20 minutes and is operating in an ambient temperature between 0° C and +40° C.
- All test equipment is in calibration.

Most tests are dependent on those that precede them, so perform all the procedures in sequential order.

Tx Electrical Pulse Shape for STM-0E (-6dB)

This test checks the cross-connect level signal amplitude directly at the TRANSMIT output connector.

Equipment Required	TDS784 Digital Scope (item 3) AMT75 75/50 ohm adapter (item 28) 75 ohm coaxial cable (item 12)
Prerequisites	All previous tests
Time Required	Approximately five minutes

1. Connect the CTS TRANSMIT output to TDS784C input as shown in Figure 4-3.

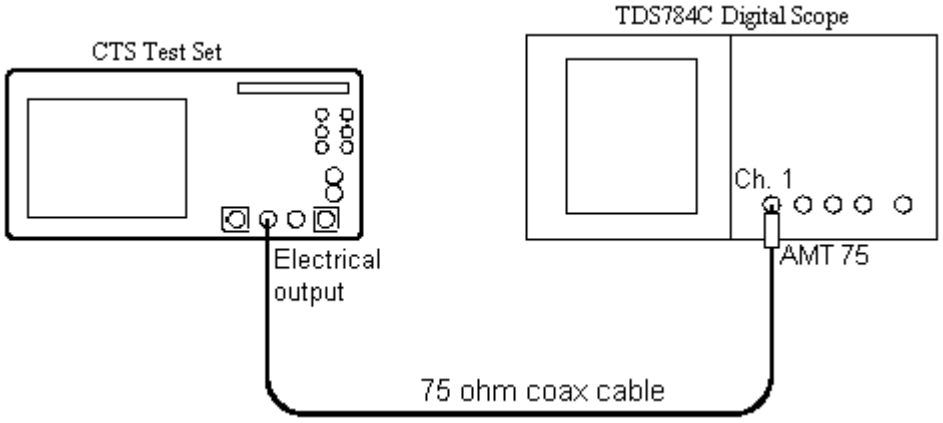


Figure 4-3: STM-0E (-6dB) Transmit Electrical Output Amplitude Hookup

2. Set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Transmit Rate	STM–0E
		Transmit Level	-6 dB

3. Perform the initial setup of the TDS784C with the following steps:

   a. Press the **DISPLAY** button and then press the button to select the **Variable Persistence**.

   b. Using the **SELECT** dial, set the Variable Persistence to **2 seconds**.

   c. Press the **TRIGGER** button and then select **Channel 1** by pressing the button.

   d. Press the **MEASURE** button and then select **Masks**.

   e. Under the **Mask Type** menu, select the **T1.102** menu item.

   f. Select the mask for **STS-1 Eye 51.84Mb/s**.

   g. Press the **AUTOSET** button.

NOTE: *Sometimes, AUTOSET is not effective for mask testing because of trigger thresholds on signals through cable having inter-symbol interference. To minimize visual effects for mask testing, adjust the trigger levels after AUTOSET.*

4. Press the button for the **Timebase Position** menu item and use the select knob to center the waveform within the mask.

Tx Electrical Amplitude and Pulse Shape for STM-0E (0dB)

This test checks the high–level signal amplitude directly at the TRANSMIT output connector.

Equipment Required	TDS784 Digital Scope (item 3) AMT75 75/50 ohm adapter (item 28) 75 ohm coaxial cable (item 12)
Prerequisites	All previous tests
Time Required	Approximately five minutes

1. Connect the CTS TRANSMIT output to TDS784C input as shown in Figure 4-4.

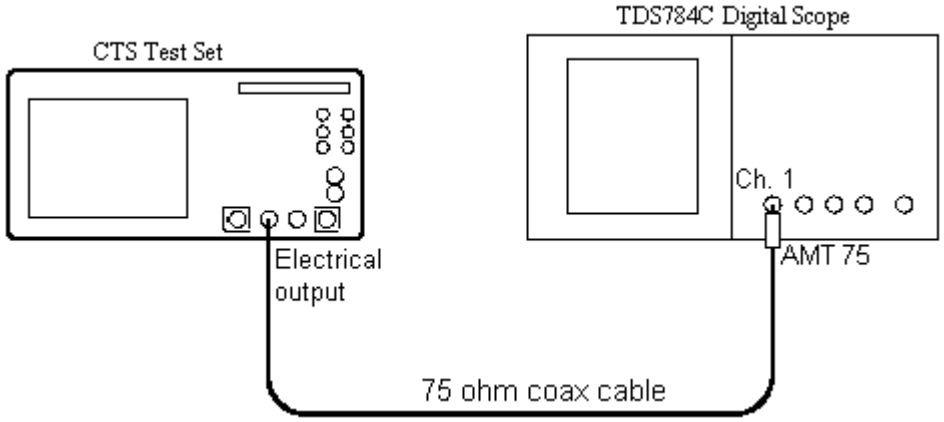


Figure 4-4: STM-0E (0dB) Transmit Electrical Output Amplitude Hookup

2. Set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Transmit Rate	STM–0E
		Transmit Level	0 dB

3. Perform the initial setup of the TDS784C with the following steps:

   a. Press the **DISPLAY** button and then press the button to select the **Variable Persistence**.

   b. Using the **SELECT** dial, set the Variable Persistence to **2 seconds**.

   c. Press the **TRIGGER** button and then select **EDGE** by pressing the button.

   d. Press the **MEASURE** button and then select **Masks**.

   e. Under the **Standard Mask** menu, select the **NONE** menu item.

   f. Press the **AUTOSET** button.

NOTE: *Sometimes, AUTOSET is not effective for mask testing because of trigger thresholds on signals through cable having inter-symbol interference. To minimize visual effects for mask testing, adjust the trigger levels after AUTOSET.*

4. Press the button for the **Timebase Position** menu item and use the select knob to center the waveform within the mask.

5. On the TDS784C digital scope, press the **CURSOR** button and select the **Horizontal bars**.

6. Move the horizontal bars so that one is at the center of the screen and one is at the top of the signal peak. The difference between these cursors is the V_{pk} value.

Tx Electrical Pulse Shape for STM-1E (-6dB)

This test checks the high–level signal amplitude directly at the TRANSMIT output connector.

Equipment Required	TDS784 Digital Scope (item 3) AMT75 75/50 ohm adapter (item 28) 75 ohm coaxial cable (item 12)
Prerequisites	All previous tests
Time Required	Approximately five minutes

1. Connect the CTS TRANSMIT output to TDS784C input as shown in Figure 4-5.

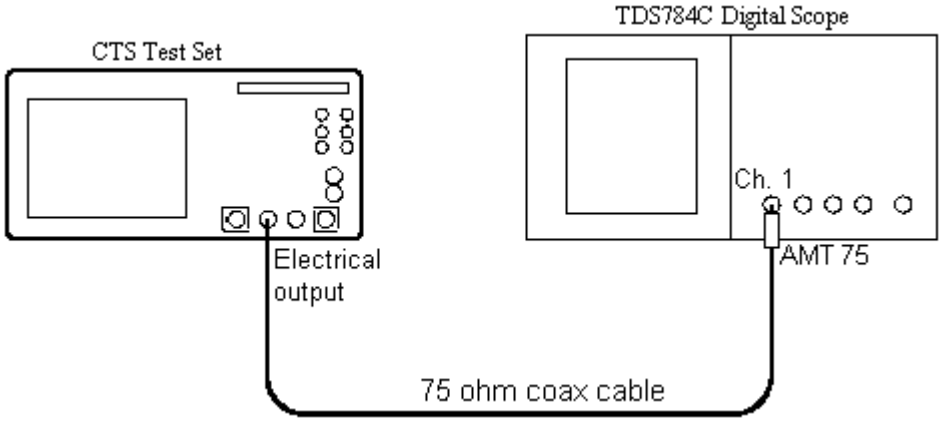


Figure 4-5: STM-1E (-6dB) Transmit Electrical Output Amplitude Hookup

2. Set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Transmit Rate	STM–1E
		Transmit Level	-6 dB

3. Perform the initial setup of the TDS784C with the following steps:

   a. Press the **DISPLAY** button and then press the button to select the **Variable Persistence**.

   b. Using the **SELECT** dial, set the Variable Persistence to **2 seconds**.

   c. Press the **TRIGGER** button and then select **Channel 1** by pressing the button.

   d. Press the **MEASURE** button and then select **Masks**.

   e. Under the **Mask Type** menu, select the **T1.102** menu item.

   f. Select the mask for **STS-3 Eye 155.52Mb/s**.

   h. Press the **AUTOSET** button.

NOTE: *Sometimes, AUTOSET is not effective for mask testing because of trigger thresholds on signals through cable having inter-symbol interference. To minimize visual effects for mask testing, adjust the trigger levels after AUTOSET.*

4. Press the button for the **Timebase Position** menu item and use the select knob to center the waveform within the mask.

Tx Electrical Pulse Shape for STM-1E (0dB)

This test checks the high–level signal amplitude directly at the TRANSMIT output connector.

Equipment Required	TDS784 Digital Scope (item 3) AMT75 75/50 ohm adapter (item 28) 75 ohm coaxial cable (item 12)
Prerequisites	All previous tests
Time Required	Approximately five minutes

1. Connect the CTS TRANSMIT output to TDS784C input as shown in Figure 4-6.

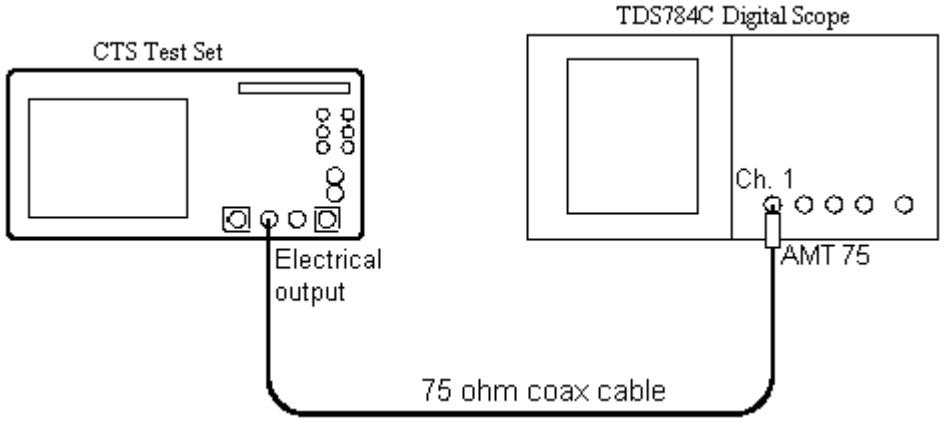


Figure 4-6: STM-1E (0dB) Transmit Electrical Output Amplitude Hookup

2. Set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Transmit Rate	STM–1E
		Transmit Level	0 dB

3. Perform the initial setup of the TDS784C with the following steps:

a. Press the **DISPLAY** button and then press the button to select the **Variable Persistence**.

b. Using the **SELECT** dial set the Variable Persistence to **2 seconds**.

c. Press the **TRIGGER** button and then select **Channel 1** by pressing the button.

d. Press the **MEASURE** button and then select **Masks**.

e. Under the **Mask Type** menu, select the **T1.102** menu item.

f. Select the mask for **STS-3 Mx Output 155.52Mb/s**.

i. Press the **AUTOSET** button.

NOTE: *Sometimes, AUTOSET is not effective for mask testing because of trigger thresholds on signals through cable having inter-symbol interference. To minimize visual effects for mask testing, adjust the trigger levels after AUTOSET.*

4. Press the button for the **Timebase Position** menu item and use the select knob to center the waveform within the mask.
5. On the TDS784C digital scope, press the **CURSOR** button and select the **Horizontal bars**.
6. Move the horizontal bars so that one is at the center of the screen and one is at the top of the signal peak. The difference between these cursors is the V_{pp} value.

Optical Output Pulse Shape for STM-0

These tests verify the signal shape of the transmitted optical output pulse by comparing with eye masks as specified in ITU G.703. These tests apply only if your CTS has one of the optional Electrical/Optical Plug–In Interface Modules installed.

Equipment Required	TDS784C Digital Scope (item 3) P6703B O/E converter (item 3) FS52 Optical Filter (item 24) Optical fiber cable (item 8)
Prerequisites	All previous Physical Layer Tests
Time Required	Approximately five minutes

1. Connect the CTS, O/E converter, optical filters, and optical fiber as shown in Figure 4-7.

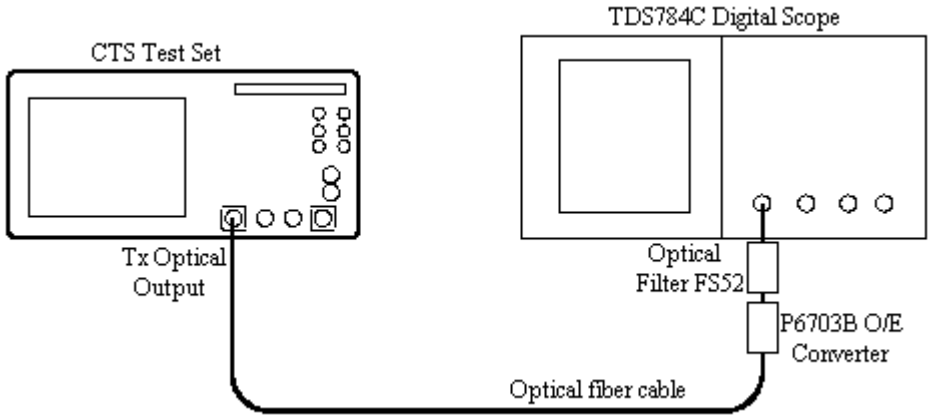


Figure 4-7: STM-0 Transmit Optical Output Pulse Shape Hookup

2. Set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Transmit Clock	INTERNAL
TRANSMIT	TRANSMIT SETTINGS	Transmit Rate	STM–0 Optical

3. Perform the initial setup of the TDS784C with the following steps:

a. Press the **DISPLAY** button and then press the button to select the **Variable Persistence**.

b. Using the **SELECT** dial set the Variable Persistence to **2 seconds**.

c. Press the **TRIGGER** button and then select **Channel 1** by pressing the button.

d. Press the **MEASURE** button and then select **Masks**.

e. Under the **Mask Type** menu, select the **SONET/SDH** menu item.

f. Select the mask for **OC1/STM0**.

g. Under **Mask Options**, select **Filter DISABLED**.

h. Press **CLEAR**, then press the **AUTOSET** button.

4. Press the button for the **Timebase Position** menu item and use the select knob to center the waveform within the mask.

Optical Output Pulse Shape for STM-1

These tests verify the signal shape of the transmitted optical output pulse by comparing with eye masks as specified in ITU G.703. These tests apply only if your CTS has one of the optional Electrical/Optical Plug–In Interface Modules installed.

Equipment Required	TDS784C Digital Scope (item 3) P6703B O/E converter (item 3) FS156 Optical Filter (item 25) Optical fiber cable (item 8)
Prerequisites	All previous Physical Layer Tests
Time Required	Approximately five minutes

1. Connect the CTS, O/E converter, optical filters, and optical fiber as shown in Figure 4-8.

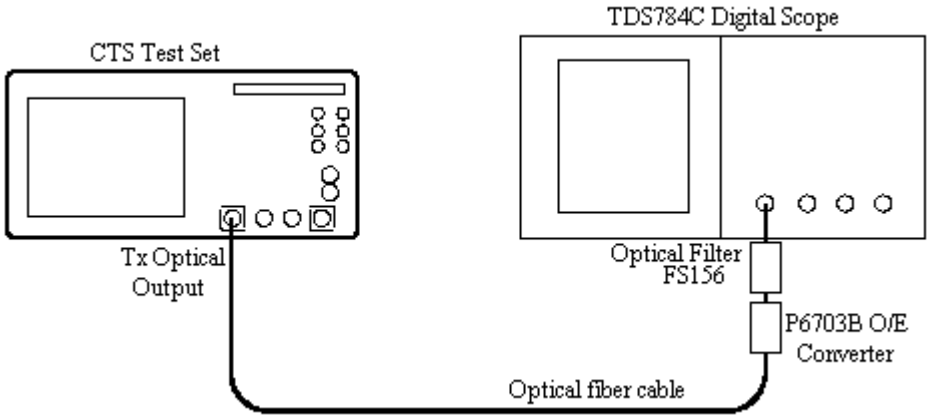


Figure 4-8: STM-1 Transmit Optical Output Pulse Shape Hookup

2. Set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Transmit Clock	INTERNAL
TRANSMIT	TRANSMIT SETTINGS	Transmit Rate	STM–1 Optical

3. Perform the initial setup of the TDS784C with the following steps:

   a. Press the **DISPLAY** button and then press the button to select the **Variable Persistence**.

   b. Using the **SELECT** dial set the Variable Persistence to **2 seconds**.

   c. Press the **TRIGGER** button and then select **Channel 1** by pressing the button.

   d. Press the **MEASURE** button and then select **Masks**.

   e. Under the **Mask Type** menu, select the **SONET/SDH** menu item.

   f. Select the mask for **OC3/STM1**.

   g. Under **Mask Options**, select **Filter DISABLED**.

   h. Press **CLEAR**, then press the **AUTOSET** button.

4. Press the button for the **Timebase Position** menu item and use the select knob to center the waveform within the mask.

Optical Output Pulse Shape for STM-4

These tests verify the signal shape of the transmitted optical output pulse by comparing with eye masks as specified in ITU G.703. These tests apply only if your CTS has one of the optional Electrical/Optical Plug–In Interface Modules installed.

Equipment Required	TDS784C Digital Scope (item 3) P6703B O/E converter (item 3) FS622 Optical Filter (item 26) Optical fiber cable (item 8)
Prerequisites	All previous Physical Layer Tests
Time Required	Approximately five minutes

1. Connect the CTS, O/E converter, optical filters, and optical fiber as shown in Figure 4-9.

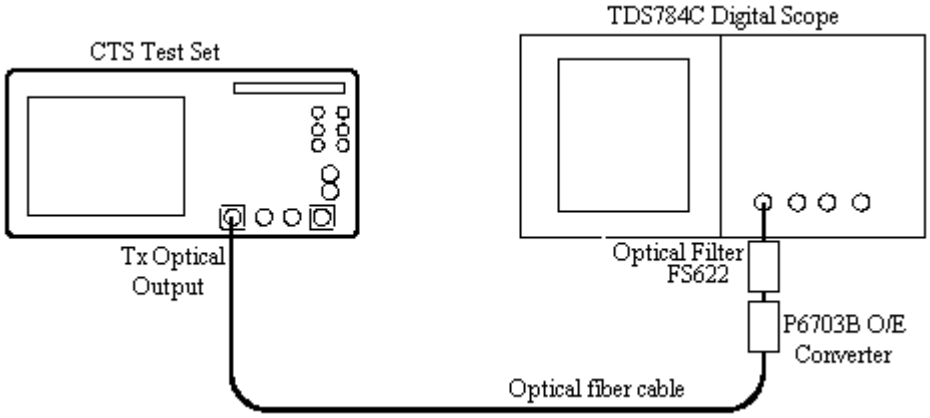


Figure 4-9: STM-4 Transmit Optical Output Pulse Shape Hookup

2. Set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Transmit Clock	INTERNAL
TRANSMIT	TRANSMIT SETTINGS	Transmit Rate	STM–4 Optical

3. Perform the initial setup of the TDS784C with the following steps:

- **a.** Press the **DISPLAY** button and then press the button to select the **Variable Persistence**.
- **b.** Using the **SELECT** dial set the Variable Persistence to **2 seconds**.
- **c.** Press the **TRIGGER** button and then select **Channel 1** by pressing the button.
- **d.** Press the **MEASURE** button and then select **Masks**.
- **e.** Under the **Mask Type** menu, select the **SONET/SDH** menu item.
- **f.** Select the mask for **OC12/STM4**.
- **g.** Under **Mask Options**, select **Filter DISABLED**.
- **h.** Press **CLEAR**, then press the **AUTOSET** button.

4. Press the button for the **Timebase Position** menu item and use the select knob to center the waveform within the mask.

Optical Power

This test verifies the power of the optical output of the CTS test set. These tests apply only if your CTS has one of the optional Electrical/Optical Plug–In Interface Modules installed.

Equipment Required	TFC200 Optical Power Meter (item 6) Optical fiber cable (item 8)
Prerequisites	All previous Physical Layer Tests
Time Required	Approximately five minutes

1. Connect the CTS, power meter, and optical fiber as shown in Figure 4-10.

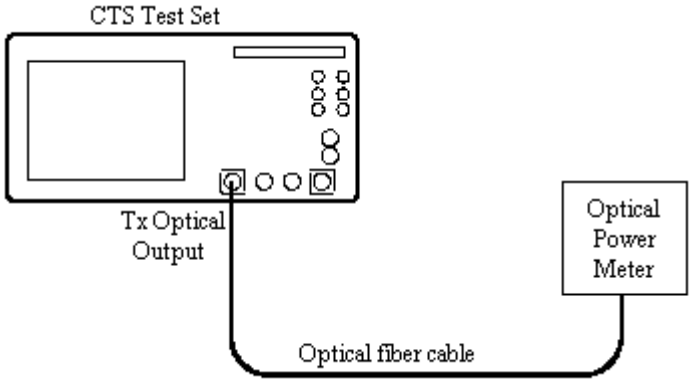


Figure 4-10: Optical Power Hookup

2. On the meter, set the wavelength as follows:

   a. If the CTS under test contains Option 03 or Option 04, set the wavelength of the meter to 1310nm.

   b. If the CTS under test contains Option 05, set the wavelength of the meter to 1550nm.

3. Set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TRANSMIT	TRANSMIT SETTINGS	TX/RX SETUP	COUPLED
TRANSMIT	TRANSMIT SETTINGS	Transmit Clock	INTERNAL
TRANSMIT	TRANSMIT SETTINGS	Transmit Rate	STM–0 Optical

4. Measure the optical power on the power meter.

5. Change the **Transmit Rate** of the CTS to **STM-1 Optical**.

6. Measure the optical power on the power meter.

7. Change the **Transmit Rate** of the CTS to **STM-4 Optical**.

8. Measure the optical power on the power meter.

Electrical Input Sensitivity

This test verifies the receiver electrical sensitivity by receiving an error–free signal at all specified levels.

Equipment Required	100 ft (31 m) length of 75 Ohm reference cable (item 10) 225 ft (68.6 m) length of 75 Ohm reference cable (item 11), two required 75 Ohm Coaxial Cable (item 12) BNC female–to–BNC female adapter (item 13), two required 10X (20 dB) Attenuator (item 17) 2X (6 dB) Attenuator (item 18)
Prerequisites	All previous Physical Layer Tests
Time Required	Approximately fifteen minutes

1. Connect the CTS TRANSMIT output through the 75 Ohm coaxial cable to the RECEIVE input as shown in Figure 4-11. You will need the additional items shown later in the procedure.

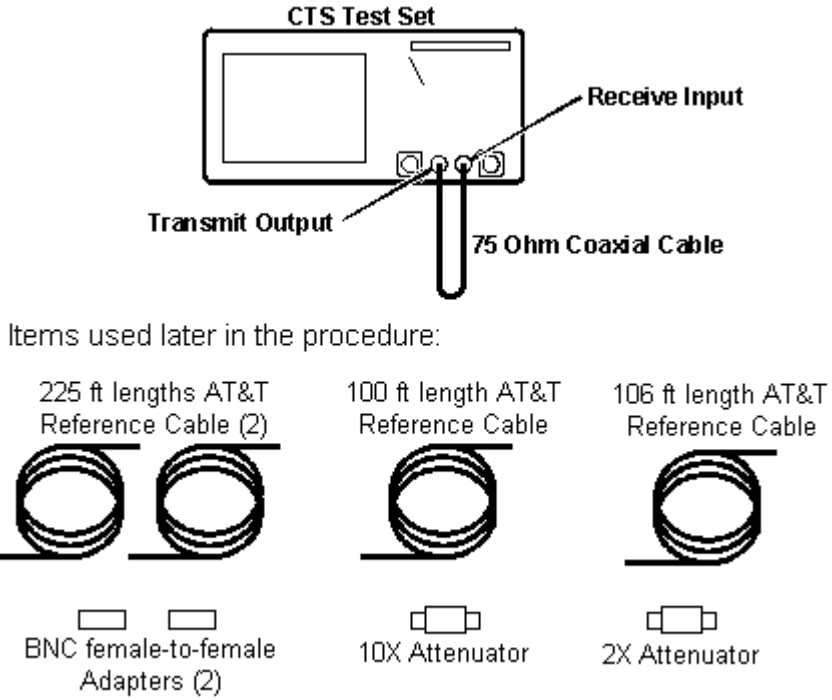


Figure 4-11: Receive Electrical Input Sensitivity Hookup

2. Perform the initial CTS setup with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TEST SETUPS	TEST CONTROL	*none*	USER DEFINED
			Minute

3. Rotate the knob to set the Test Duration to **2 m**, and then press **Done**.

4. **Part 1:** To verify the STM–1E, 0dB sensitivity, set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TRANSMIT	TRANSMIT SETTINGS	Transmit Rate	STM–1E
		Transmit Level	0 dB
RECEIVE	RECEIVE SETTINGS	Receive Rate	STM–1E
		Receive Level	0 dB
RESULTS	MAIN RESULTS	*none*	Errors

5. Press the **START/STOP** button and verify that the START/STOP light is on.

6. Wait two minutes for the test to complete. When the START/STOP light turns off, verify that all ERROR RATIOS shown in the MAIN RESULTS page are either 0.00 or less than 10^{-10}.

7. **Part 2:** Install the 2X attenuator in series with the coaxial cable between the TRANSMIT output and the RECEIVE input.

8. Press the **START/STOP** button, and verify that the START/STOP light is on.

9. Wait two minutes for the test to complete. When the START/STOP light turns off, verify that all ERROR RATIOS shown in the MAIN RESULTS page are either 0.00 or less than 10^{-10}.

10. To verify the STM–1E, -6dB sensitivity, set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TRANSMIT	TRANSMIT SETTINGS	Transmit Level	0 dB
RECEIVE	RECEIVE SETTINGS	Receive Level	-6 dB
RESULTS	MAIN RESULTS	*none*	Errors

11. Install one 225 ft (68.6 m) length of reference cable and one 100 ft (31 m) length of reference cable (325 ft or 100 m, total) between the TRANSMIT output and the RECEIVE input (no attenuators).

12. Press the **START/STOP** button and verify that the START/STOP light is on.

13. Wait two minutes for the test to complete. When the START/STOP light turns off, verify that all ERROR RATIOS shown in the MAIN RESULTS page are either 0.00 or less than 10^{-10}.

14. To verify the **STM–1E**, –12dB sensitivity, set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TRANSMIT	TRANSMIT SETTINGS	Transmit Level	0 dB
RECEIVE	RECEIVE SETTINGS	Receive Level	-12 dB
RESULTS	MAIN RESULTS	*none*	Errors

15. Install two 225 ft (68.6 m) lengths of reference cable and one 100 ft (31 m) length of reference cable (550 ft or 168 m, total) between the TRANSMIT output and the RECEIVE input (no attenuators).

16. Press the **START/STOP** button and verify that the START/STOP light is on.

17. Wait two minutes for the test to complete. When the START/STOP light turns off, verify that all ERROR RATIOS shown in the MAIN RESULTS page are either 0.00 or less than 10^{-10}.

18. To verify the **monitor–level** sensitivity for STM-1E, set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TRANSMIT	TRANSMIT SETTINGS	Transmit Level	High or 0 dB
RECEIVE	RECEIVE SETTINGS	Receive Level	Monitor
RESULTS	MAIN RESULTS	*none*	Errors

19. Remove the three reference cables. Install a 10X attenuator and a 2X attenuator (26dB total attenuation) in series with the short (≈1 m) length of 75 Ohm coaxial cable between the TRANSMIT output and the RECEIVE input.

20. Press the **START/STOP** button and verify that the START/STOP light is on.

21. Wait two minutes for the test to complete. When the START/STOP light turns off, verify that all ERROR RATIOS shown in the MAIN RESULTS SDH anomalies page are either 0.00 or less than 10^{-10}.

22. Part 1: To verify the STM–0E, 0dB sensitivity, set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TRANSMIT	TRANSMIT SETTINGS	Transmit Rate	STM–0E
		Transmit Level	0 dB
RECEIVE	RECEIVE SETTINGS	Receive Rate	STM–0E
		Receive Level	0 dB
RESULTS	MAIN RESULTS	*none*	Errors

23. Press the **START/STOP** button and verify that the START/STOP light is on.

24. Wait two minutes for the test to complete. When the START/STOP light turns off, verify that all ERROR RATIOS shown in the MAIN RESULTS page are either 0.00 or less than 10^{-10}.

25. Part 2: Install the 2X attenuator in series with the coaxial cable between the TRANSMIT output and the RECEIVE input.

26. Press the **START/STOP** button, and verify that the START/STOP light is on.

27. Wait two minutes for the test to complete. When the START/STOP light turns off, verify that all ERROR RATIOS shown in the MAIN RESULTS page are either 0.00 or less than 10^{-10}.

28. To verify the STM–0E, -6dB sensitivity, set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TRANSMIT	TRANSMIT SETTINGS	Transmit Level	0 dB
RECEIVE	RECEIVE SETTINGS	Receive Level	-6 dB
RESULTS	MAIN RESULTS	*none*	Errors

29. Install two 225 ft (68.6 m) length of reference cable and one 100 ft (31 m) length of reference cable (550 ft or 168 m, total) between the TRANSMIT output and the RECEIVE input (no attenuators).

30. Press the **START/STOP** button and verify that the START/STOP light is on.

31. Wait two minutes for the test to complete. When the START/STOP light turns off, verify that all ERROR RATIOS shown in the MAIN RESULTS page are either 0.00 or less than 10^{-10}.

32. To verify the **STM–0E**, –12dB sensitivity, set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TRANSMIT	TRANSMIT SETTINGS	Transmit Level	0 dB
RECEIVE	RECEIVE SETTINGS	Receive Level	-12 dB
RESULTS	MAIN RESULTS	*none*	Errors

33. Install two 225 ft (68.6 m) lengths of reference cable and one 100 ft (31 m) length of reference cable and one 106 ft cable (656 ft or 201 m, total) between the TRANSMIT output and the RECEIVE input (no attenuators).

34. Press the **START/STOP** button and verify that the START/STOP light is on.

35. Wait two minutes for the test to complete. When the START/STOP light turns off, verify that all ERROR RATIOS shown in the MAIN RESULTS page are either 0.00 or less than 10^{-10}.

36. To verify the **monitor–level** sensitivity for STM-0E, set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TRANSMIT	TRANSMIT SETTINGS	Transmit Level	High or 0 dB
RECEIVE	RECEIVE SETTINGS	Receive Level	Monitor
RESULTS	MAIN RESULTS	*none*	Errors

37. Remove the three reference cables. Install a 10X (20dB) attenuator in series with two 225ft cables and a 100ft cable between the TRANSMIT output and the RECEIVE input.

38. Press the **START/STOP** button and verify that the START/STOP light is on.

39. Wait two minutes for the test to complete. When the START/STOP light turns off, verify that all ERROR RATIOS shown in the MAIN RESULTS SDH anomalies page are either 0.00 or less than 10^{-10}.

Optical Input Sensitivity

These tests verify the sensitivity of the optical receiver. These tests apply only if your CTS has one of the optional Electrical/Optical Plug–In Interface Modules installed.

Equipment Required	Optical attenuator (item 5) Optical Power Meter (item 6) Optical fiber cable (item 8), two required
Prerequisites	All previous Physical Layer Tests
Time Required	Approximately thirty minutes

1. Connect the CTS TRANSMIT output through the optical attenuator to the SDH/SONET Reference Receiver and Power Meter as shown in Figure 4-12.

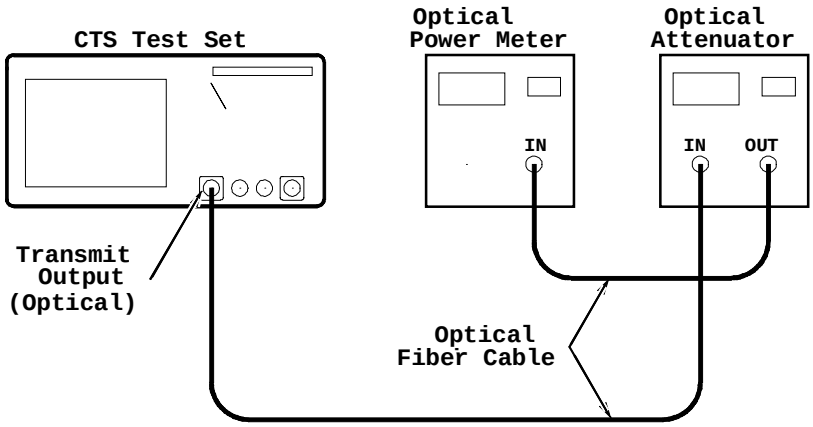


Figure 4-12: Receive Optical Input Sensitivity Hookup

2. Perform the initial CTS setup with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TEST SETUPS	TEST CONTROL	*none*	USER DEFINED
			Minute

3. Rotate the knob to set the Test Duration to **2 m**, and then press **Done**.

4. Set the optical power meter measurement units to **dBm**.

5. If your CTS has Option 03 or Option 04, set the optical attenuator and optical power meter wavelengths to **1310 nm**. If your CTS has Option 05, set the optical attenuator and optical power meter wavelengths to **1550 nm**.

6. To verify the STM–1 sensitivity, set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TRANSMIT	TRANSMIT SETTINGS	Transmit Rate	STM–1 Optical
		Tx/Rx Settings	Coupled
RESULTS	MAIN RESULTS	*none*	Errors

7. Set the optical attenuator attenuation so that the optical power meter reading is **-28 dBm**.

8. Remove the fiber connection from the optical power meter, and connect it to the RECEIVE input of the CTS.

9. Perform the test with the following steps:

   a. Press the **START/STOP** button and verify that the START/STOP light is on.

   b. Wait two minutes for the test to complete; the START/STOP light turns off when the test is complete.

   c. Verify that all measured ERROR RATIOS are 0.00 or less than 10^{-10}.

10. Remove the fiber connection from the RECEIVE input of the CTS, and connect it to the optical power meter.

11. To verify the STM–0 Optical sensitivity, set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TRANSMIT	TRANSMIT SETTINGS	Transmit Rate	STM–0 Optical
		Tx/Rx Settings	Coupled
RESULTS	MAIN RESULTS	*none*	Errors

12. Set the optical attenuator attenuation so that the optical power meter reading is **-28 dBm**.

13. Remove the fiber connection from the optical power meter, and connect it to the RECEIVE input of the CTS.

14. Perform the test with the following steps:

a. Press the **START/STOP** button and verify that the START/STOP light is on.

b. Wait two minutes for the test to complete; the START/STOP light turns off when the test is complete.

c. Verify that all measured ERROR RATIOS are 0.00 or less than 10^{-10}.

15. Remove the fiber connection from the RECEIVE input of the CTS, and connect it to the optical power meter.

16. If your CTS does not have STM–4 capability (option 04), proceed to *Check Internal Clock Accuracy*. To verify the STM–4 sensitivity, set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TRANSMIT	TRANSMIT SETTINGS	Transmit Rate	STM–4
RESULTS	MAIN RESULTS	*none*	Errors

17. Set the optical attenuator attenuation so that the optical power meter reading is **-28 dBm**.

18. Remove the fiber connection from the optical power meter, and connect it to the RECEIVE input of the CTS.

19. Perform the test with the following steps:

a. Press the **START/STOP** button, and verify that the START/STOP light is on.

b. Wait two minutes for the test to complete; the START/STOP light turns off when the test is complete.

c. Verify that all measured ERROR RATIOS are 0.00 or less than 10^{-10}.

Internal Clock Accuracy

This test verifies the accuracy of the internal clock at its base frequency of 51.84 MHz. All internally generated transmit clock rates are derived from exact harmonics (1x, 3x, or 12x) of this base frequency. Therefore, the accuracy of all transmit line rates are indirectly verified by this test.

Equipment Required	Universal Counter/Timer (item 1) 50 Ohm SMB–to–BNC coaxial cable (item 15)
Prerequisites	All previous Physical Layer Tests
Time Required	Approximately ten minutes

1. Connect the CAL output (CTS rear panel) to the Universal Counter/Timer input as shown in Figure 4-13.

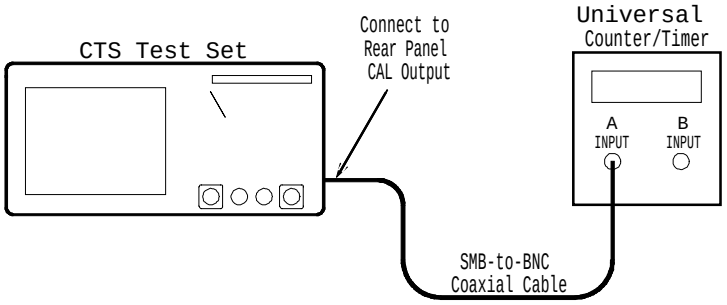


Figure 4-13: Internal Clock Accuracy Hookup

2. To verify the internal clock accuracy, set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup

3. Make the following settings on the Universal Counter/Timer:
   a. Set input impedance to **50 Ohm**.
   b. Set input coupling to **AC**.
   c. If you are using a Tektronix DC5010 counter, set the averages to 10. If you are using an HP53131A counter, set **DIGITS** to **8** (refer to the *HP53131A/132A Universal Counter Operating Guide*, pages 1–5, 2–7, 2–8, and 2–16, for instructions on how to set **DIGITS**).
   d. Set measurement mode to **Frequency**.
4. Verify that the Universal Counter/Timer reads between 51,839,762 Hz and 51,840,238 Hz (inclusive).

Transmit Line Frequency Offset

This test verifies the transmit line frequency offset at the line rate of 51.84 MHz. The frequency offset of all transmit line rates is indirectly verified by this test.

Equipment Required	Universal Counter/Timer (item 1) 50 Ohm SMB–to–BNC coaxial cable (item 15)
Prerequisites	All previous Physical Layer Tests
Time Required	Approximately ten minutes

1. Connect the CAL output (CTS rear panel) to the Universal Counter/Timer input as shown in Figure 4-14 (same setup as previous test).

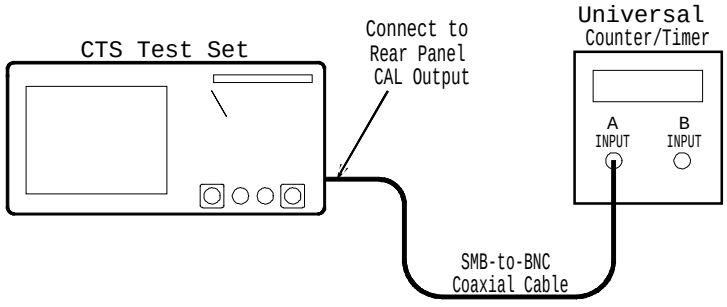


Figure 4-14: Transmit Line Frequency Offset Hookup

2. To verify the transmit line frequency offset, set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	POINTERS & TIMING	Pointer/Timing Mode	Frequency Offset
		Frequency Offset	MAX +100 ppm

3. Make the following settings on the Universal Counter/Timer:
   a. Set input impedance to **50 Ohm**.
   b. Set input coupling to **AC**.
   c. If you are using a Tektronix DC5010 counter, set the averages to 108. If you are using an HP53131A counter, set **DIGITS** to **8** (refer to the *HP53131A/132A Universal Counter Operating Guide*, pages 1–5, 2–7, 2–8, and 2–16, for instructions on how to set **DIGITS**).
   d. Set measurement mode to **Frequency**.
4. Verify that the Universal Counter/Timer reads between 51,844,946 Hz and 51,845,422 Hz (inclusive).
5. To test negative transmit line frequency offset, change the CTS setup with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TRANSMIT	POINTERS & TIMING	Frequency Offset	USER DEFINED
		Frequency Offset	Coarse

6. Rotate the knob to set the Frequency Offset to **-100 ppm**, and then press **Done**.
7. Verify that the Universal Counter/Timer reads between 51,834,578 Hz and 51,835,054 Hz (inclusive).

Option 38 (and Option 55) Performance Verification

Throughout this procedure the word **"CTS (Under Test)"** refers to the CTS that you are verifying. The word **"TEST CTS"** is the CTS that will be used to test the CTS being verified.

PDH MUX/Demux

To perform each of the PDH Mux/Demux tests the CTS under test must have its PDH and 2 Mb/s inputs and outputs connected. With a 75-ohm cable (item 12), connect the 75 Ohm PDH output to the 75 Ohm PDH input. Using a 120-ohm cable (item 16), connect the 2Mb/s output to the 2Mb/s input.

2Mb/s (Balanced)

Setup CTS (Under Test) Transmit Settings

TX RATE **= 2Mb/s HDB3 (Bal).**
TX Clock **= Internal**
Line Clock **Offset = 0.0 PPM**
***** Payload **= 2Mb/s PCM31**
Test Pattern **= PRBS 2^23-1 normal**
TX/RX Setup **= Coupled**

Verify CTS (Under Test) "Signal Present" and "Pattern Lock" LEDs are lit.

1. Press "Start Stop" on the front panel. Verify the START indicator is lit.
2. Press the "results" button on the front panel.
3. Select "Test Summary".

Verify that there are "No Alarms" and "No Errors".

4. Press the "Transmit" button on the front panel.
5. Select "Defect & Anomalies".
6. Highlight the "Error Type set to" and select "Pattern Bit".
7. Press the "Insert Error" button on the front panel 5 times.
8. Press the "Results" button on the front panel.
9. Select "Test Summary".
10. Verify "Pattern Bit Errors" = 5. Press "Start Stop" and "Clear History".

8 Mb/s (Unbalanced)

Setup CTS (Under Test) Transmit Settings

TX RATE **= 8Mb/s HDB3**
TX Clock **= Internal**
Line Clock **Offset = 0.0ppm**
***** Payload **= 8Mb/s framed**
Test Pattern **= PRBS 2^23-1 normal**
TX/RX Setup **= Coupled**

Verify CTS (Under Test) "Signal Present" and "Pattern Lock" LEDs are lit.

1. Press "Start Stop" on the front panel. Verify START indicator is lit.
2. Press the "Results" button on the front panel.
3. Select "Test Summary".

Verify that there are "No Alarms" and "No Errors".

1. Press the "Transmit" button on the front panel.
2. Select "Defect & Anomalies".
3. High light the "Error Type set to" and select "Pattern Bit".
4. Press the "Insert Error" button on the front panel 5 times.
5. Press the "Results" button on the front panel.
6. Select "Test Summary".
7. Verify "Pattern Bit Errors" = 5. Press "Start Stop" and "Clear History".

34Mb/s MUX/Demux

Setup CTS (Under Test) Transmit Settings

TX Rate = **34Mb/s HDB3**
TX Clock = **Internal**
Line Clock Offset = **0.0ppm**
***Payload = **34Mb/s Framed**
Test Pattern = **PRBS 2^23-1 normal**
TX/RX Setup = **Coupled**

Verify CTS (Under Test) "Signal Present" and "Pattern Lock" LEDs are lit.

1. Press the "Start Stop" button on the front panel.
2. Press the "results" button on the front panel.
3. Select "Test Summary".

Verify that there are "No Alarms" and "No Errors".

1. Press the "Transmit" button on the front panel.
2. Select "Defect & Anomalies".
3. High light the "Error Type set to" and select "Pattern Bit".
4. Press the "Insert Error" button on the front panel 5 times.
5. Press the "Results" button on the front panel.
6. Select "Test Summary".
7. Verify "Pattern Bit Errors" = 5. Press "Start Stop" and "Clear History".
8. Repeat the above steps with the payload = 8Mb/s Framed; then repeat again with the payload = 2Mb/s PCM31.
9. Press "Start Stop" and "Clear History".

Option 55 Only

45Mb/s

Setup CTS (Under Test) Transmit Settings

TX Rate = **45Mb/s B3ZS**
TX Clock = **Internal**
Line Clock Offset = **0.0ppm**
***Payload = **45 Mb/s Unframed**
Test Pattern = **PRBS 2^23-1 normal**
TX/RX Setup = **Coupled**

Verify CTS (Under Test) "Signal Present" and "Pattern Lock" LEDs are lit.

1. Press the "Start Stop" button on the front panel.
2. Press the "results" button on the front panel.
3. Select "Test Summary".

Verify that there are "No Alarms" and "No Errors".

4. Press the "Transmit" button on the front panel.
5. Select "Defect & Anomalies".
6. High light the "Error Type set to" and select "Pattern Bit".
7. Press the "Insert Error" button on the front panel 5 times.
8. Press the "Results" button on the front panel.
9. Select "Test Summary".
10. Verify "Pattern Bit Errors" = 5. Press "Start Stop" and "Clear History".
11. Repeat the above steps with the payload = M13 Framed; then repeat again with the payload = C-BIT Framed.
12. Press "Start Stop" and "Clear History".

140Mb/s MUX/ Demux

Setup CTS (Under Test) Transmit Settings

TX Rate = **140Mb/s.**
TX Clock = **Internal**
Line Clock Offset = **0.0ppm**
***** Payload = **140Mb/s Framed**
Test Pattern = **PRBS 2^23-1 normal**
TX/RX Setup = **Coupled**

Verify CTS (Under Test) "Signal Present" and "Pattern Lock" LEDs are lit.

1. Press the "Start Stop" button on the front panel.
2. Press the "results" button on the front panel.
3. Select "Test Summary".

Verify that there are "No Alarms" and "No Errors".

1. Press the "Transmit" button on the front panel.
2. Select "Defect & Anomalies".
3. High light the "Error Type set to" and select "Pattern Bit".
4. Press the "Insert Error" button on the front panel 5 times.
5. Press the "Results" button on the front panel.
6. Select "Test Summary".
7. Verify "Pattern Bit Errors" = 5
8. Repeat the above tests with the payload = 34Mb/s Unframed; then again with the payload = 8Mb/s Framed; then again with the payload = 2Mb/s PCM31.
9. Press "Test Setup", then "Recall Instrument Setups". Select "Recall Setup".

External Add/Drop

CTS Cable Connections

Connect a 75 Ohm cable (item 12) from **CTS (Under Test)** 75 Ohm 52/155/622 Mb/s output to the 75 Ohm 52/155/622 Mb/s input of the **CTS (Under Test)**.

Connect a 75 Ohm cable (item 12) from **CTS (Under test)** 75 Ohm 2/8/34/140 Mb/s input, to the **TEST CTS** (item 4) 75 Ohm 2/8/34/140 Mb/s output.

Connect a 75 Ohm cable (item 12) from **CTS (Under test)** 75 Ohm 2/8/34/140 Mb/s output, to the **TEST CTS** (item 4) 75 Ohm 2/8/34/140 Mb/s input.

Connect a 120 Ohm cable (item 16) from **CTS (Under test)** 2Mb/s 120 Ohm input, to the **TEST CTS** (item 4) 2Mb/s 120 Ohm output.

Connect a 120 Ohm cable (item 16) from **CTS (Under test)** 2Mb/s 120 Ohm output, to the **TEST CTS** (item 4) 2Mb/s 120 Ohm input.

2Mb/s TU-12 External Add/Drop (Balanced)

Setup the CTS (Under Test)

Transmitter	Receiver
TX Rate = **STM-1 Electrical**	RX Rate = **STM-1 Electrical**
TX Clock = **Internal**	RX Level = **-6dB**
TX Level = **-6dB**	TU Under Test **= 1**
Structure = **TU12 Floating Async**	Structure = **TU12 Floating Async**
TU Under Test **= All TU12s**	TU Under Test = **TUG3:1 TUG2:1 TU12:1**
Payload **= 2Mb/s.....Ext Add (Bal)**	Payload **= 2Mb/s PCM31**
Ext Add Input Level = **Normal (Cross Connect)**	Test Pattern **= PRBS 2^23-1 normal**
TX/RX Setup = **Coupled**	Payload Drop = **2Mb/s Balanced**

Setup the TEST CTS (bench scope)

Transmitter	Receiver
TX Rate **= 2Mb/s HDB3 (Bal)**	RX Rate = **2Mb/s HDB3 (Bal)**
TX Clock **= Internal**	Receive Level = **Normal (Cross Connect)**
Line Clock Offset **= 0.0ppm**	Payload = **2Mb/s PCM31**
Payload **= 2Mb/s PCM31**	Test Pattern = **PRBS 2^23-1 normal**
Test Pattern **= PRBS 2^23-1 normal**	

TX/RX Setup **= Coupled**	

Verify CTS (Under Test) and TEST CTS "Signal Present and "Pattern Lock" LEDs are lit.

1. Press the "Start Stop" button on the front panel of both CTS units so the Start indicators are lit.
2. Press the "results" button on the front panel of both CTS units.
3. Select "Test Summary" on both CTS units.

Verify that there are "No Alarms" and "No Errors" on both CTS units.

1. Disconnect the 120 Ohm cable from the CTS (Under Test) "2Mb/s input".
2. Verify CTS (Under Test) red "LOF" led is lit.
3. Verify TEST CTS "LOF" and red "ERROR" LEDs are lit.
4. Reconnect the 120 Ohm cable to the CTS (Under Test) 120 Ohm "2Mb/s input". Clear errors on both CTS units (Test and Under Test).
5. Disconnect the 75 Ohm cable from the CTS (Under Test) 75 Ohm 52/155/622 Mb/s input.
6. Verify CTS (Under Test) red "LOS" led is lit.
7. Verify TEST CTS "LOF" and red "ERROR" LEDs are lit.
8. Reconnect the 75 Ohm cable to the **CTS (Under Test)** 75 Ohm 52/155/622 Mb/s input. Clear errors on both CTS units (Test and Under Test).

Verify CTS (Under Test) and TEST CTS "Signal Present" and "pattern lock" LEDs are lit.

1. Press the "Start Stop" button on the front panel of both CTS units twice.
2. Press the "results" button on the front panel of both CTS units.
3. Select "Test Summary" on both CTS units.

Verify that there are "No Alarms" and "No Errors" on both CTS units.

TEST CTS Setup

1. Press the "Transmit" button on the front panel.
2. Select "Defect & Anomalies".
3. High light the "Error Type set to" and select "Pattern Bit".
4. Press the "Insert Error" button on the front panel 5 times.
5. Press the "Results" button on the front panel.

6. Select “Test Summary”.
7. Verify “Pattern Bit Errors” = 5

CTS (Under Test)

1. Verify “Pattern Bit Errors” = 5
2. Clear errors on both CTS units (Test and Under Test).

2Mb/s TU-12 External Add/Drop (Unbalanced)

Setup CTS (Under Test)

Transmitter	Receiver
TX Rate = **STM-1 Electrical**	RX Rate **= STM-1 Electrical**
TX Clock = **Internal**	Receive Level = **-6dB**
TX Level = **-6dB**	Structure = **TU12 Floating Async**
Structure = **TU12 Floating Async**	TU Under Test = **TUG3:1 - TUG12:1**
TU Under Test **= All TU12s**	Payload **= 2Mb/s PCM31**
Payload **= 2Mb/s.....Ext Add (Unbal)**	Test Pattern **= PRBS 2^23-1 normal**
Ext Add Input Level = **Normal (Cross Connect)**	Payload Drop = **2Mb/s (Unbalanced)**
TX/RX Setup = **Coupled**	TX/RX Setup = **Coupled**

Setup the TEST CTS

Transmitter	Receiver
TX Rate **= 2Mb/s HDB3 (Unbal)**	RX Rate = **2Mb/s HDB3 (Unbal)**
TX Clock **= Internal**	Receive Level = **Normal (Cross Connect)**
Line Clock Offset **= 0.0ppm**	Payload = **2Mb/s PCM31**
Payload **= 2Mb/s PCM31**	Test Pattern = **PRBS 2^23-1**
Test Pattern **= PRBS 2^23-1**	TX/RX Setup **= Coupled**
TX/RX Setup **= Coupled**	

Verify CTS (Under Test) and TEST CTS “Signal Present and “Pattern Lock” LEDs are lit.

1. Press the “Start Stop” button on the front panel of both CTS units so both Start indicators are lit.
2. Press the “results” button on the front panel of both CTS units.
3. Select “Test Summary” on both CTS units.

Verify that there are "No Alarms" and "No Errors" on both CTS units.

1. Disconnect the 75 Ohm cable from the **CTS (Under Test)** 75 Ohm 2/8/34/140 Mb/s input.
2. Verify CTS (Under Test) "LOF" led is lit.
3. Verify TEST CTS "LOF" and "ERROR" LEDs are lit.
4. Reconnect the 75 Ohm cable to the CTS (Under Test) 75 Ohm 2/8/34/140 Mb/s input.
5. Disconnect the 75 Ohm cable from the CTS (Under Test) 75 Ohm 52/155/622 Mb/s input.
6. Verify CTS (Under Test) red "LOS" led is lit.
7. Verify TEST CTS red "LOF", red PDH-AIS, and red "ERROR" LEDs are lit. Press "Start Stop" and "Clear History" on both CTS units (Test and Under Test).
8. Reconnect the 75 Ohm cable to the **CTS (Under Test)** 75 Ohm STM input.

Verify CTS (Under Test) and TEST CTS "Signal Present" and "pattern lock" LEDs are lit.

9. Press the "Start Stop" button on the front panel of both CTS units .
10. Press the "results" button on the front panel of both CTS units..
11. Select "Test Summary" on both CTS units.
12. Verify that there are no "Alarms or Errors" on both CTS units.

TEST CTS Setup

13. Press the "Transmit" button on the front panel.
14. Select "Defect & Anomalies".
15. High light the "Error Type set to" and select "Pattern Bit".
16. Press the "Insert Error" button on the front panel 5 times.
17. Press the "Results" button on the front panel.
18. Select "Test Summary".
19. Verify "Pattern Bit Errors" = 5

CTS (Under Test)

20. Verify "Pattern Bit Errors" = 5
21. Press "Start Stop" and "Clear History" on both CTS units.

34Mb/s TU-3 External Add/Drop

Setup the CTS (Under Test)

Transmitter	Receiver
TX Rate = **STM-1 Electrical**	RX Rate **= STM-1 Electrical**
TX Clock = **Internal**	Receive Level **= -6dB**
TX Level = **-6dB**.	
Structure = **TU3 Floating Async**	Structure **= TU3 Floating Async**
TU Under Test **= All TU3s.**	TU Under Test **= TU3 :1**
Payload **= 34Mb/s External Add**	Payload **= 34Mb/s Framed.**
Ext Add Input Level = **Normal (Cross Connect)**	Test Pattern = **PRBS 2^23-1 normal**
TX/RX Setup = **Coupled**	Payload Drop **= Drop 34Mb/s**
	TX/RX Setup **= Coupled**

Setup the TEST CTS

Transmitter	Receiver
TX Rate **= 34Mb/s HDB3**	RX Rate = **34Mb/s HDB3**
TX Clock **= Internal**	Receive Level = **Normal (Cross Connect)**
Line Clock Offset **= 0.0ppm**	Payload = **34Mb/s Framed**
Payload **= 34Mb/s framed**	Test Pattern = **PRBS 2^23-1**
Test Pattern **= PRBS 2^23-1**	TX/RX Setup **= Coupled**
TX/RX Setup **= Coupled**	

Verify CTS (Under Test) and TEST CTS "Signal Present and "Pattern Lock" LEDs are lit.

1. Press the "Start Stop" button on the front panel of both CTS units.
2. Press the "results" button on the front panel of both CTS units.
3. Select "Test Summary" on both CTS units.

Verify that there are "No Alarms" and "No Errors" on both CTS units.

1. Disconnect the 75 Ohm cable from the CTS (Under Test) 75 Ohm PDH input.
2. Verify CTS (Under Test) "LOF" led is lit.
3. Verify TEST CTS "LOF" and "ERROR" LEDs are lit.
4. Reconnect the 75 Ohm cable to the CTS (Under Test) 75 Ohm PDH input.
5. Disconnect the 75 Ohm cable from the CTS (Under Test**)** 75 Ohm STM input.

Verify CTS (Under Test) red "LOS" led is lit.

Verify TEST CTS red "LOF" and red "ERROR" LEDs are lit.

1. Reconnect the 75 Ohm cable to the **CTS (Under Test)** 75 Ohm STM input.
2. Press "Start Stop" and "Clear History" on both CTS.

Verify CTS (Under Test) and TEST CTS "Signal Present" and "pattern lock" LEDs are lit.

1. Press the "Start Stop" button on the front panel of both CTS units .
2. Press the "results" button on the front panel of both CTS units..
3. Select "Test Summary" on both CTS units.

Verify that there are no "Alarms or Errors" on both CTS units.

TEST CTS Setup

1. Press the "Transmit" button on the front panel.
2. Select "Defect & Anomalies".
3. High light the "Error Type set to" and select "Pattern Bit".
4. Press the "Insert Error" button on the front panel 5 times.
5. Press the "Results" button on the front panel.
6. Select "Test Summary".
7. Verify "Pattern Bit Errors" = 5

CTS (Under Test)

1. Verify "Pattern Bit Errors" = 5
2. Press "Start Stop" and "Clear History" on both units.

Option 55 Only

45Mb/s TU-3 External Add/Drop

Setup the CTS (Under Test)

Transmitter	Receiver
TX Rate = **STM-1 Electrical**	RX Rate **= STM-1 Electrical**
TX Clock = **Internal**	Receive Level **= -6dB**
TX Level = **-6dB**.	
Structure = **TU3 Floating Async**	Structure **= TU3 Floating Async**
TU Under Test **= All TU3s.**	TU Under Test **= TU3 :1**
Payload **= 45Mb/s External Add**	Payload **= 45Mb/s C-BIT**
Ext Add Input Level = **Normal (Cross Connect)**	Test Pattern = **PRBS 2^23-1 normal**
TX/RX Setup = **Coupled**	Payload Drop **= Drop 45Mb/s B3ZS**
	TX/RX Setup **= Coupled**

Setup the TEST CTS

Transmitter	Receiver
TX Rate **= 45Mb/s B3ZS**	RX Rate = **45Mb/s B3ZS**
TX Clock **= Internal**	Receive Level = **Normal (Cross Connect)**
Line Clock Offset **= 0.0ppm**	Payload = **45Mb/s C-BIT**
Payload **= 45Mb/s C-BIT**	Test Pattern = **PRBS 2^23-1**
Test Pattern **= PRBS 2^23-1**	TX/RX Setup **= Coupled**
TX/RX Setup **= Coupled**	

Verify CTS (Under Test) and TEST CTS "Signal Present and "Pattern Lock" LEDs are lit.

4. Press the "Start Stop" button on the front panel of both CTS units.
5. Press the "results" button on the front panel of both CTS units.
6. Select "Test Summary" on both CTS units.

Verify that there are "No Alarms" and "No Errors" on both CTS units.

6. Disconnect the 75 Ohm cable from the CTS (Under Test) 75 Ohm PDH input.
7. Verify CTS (Under Test) "LOF" led is lit.
8. Verify TEST CTS "LOF" and "ERROR" LEDs are lit.
9. Reconnect the 75 Ohm cable to the CTS (Under Test) 75 Ohm PDH input.
10. Disconnect the 75 Ohm cable from the CTS (Under Test**)** 75 Ohm STM input.

Verify CTS (Under Test) red "LOS" led is lit.

Verify TEST CTS red "LOF" and red "ERROR" LEDs are lit.

3. Reconnect the 75 Ohm cable to the **CTS (Under Test)** 75 Ohm STM input.
4. Press "Start Stop" and "Clear History" on both CTS.

Verify CTS (Under Test) and TEST CTS "Signal Present" and "pattern lock" LEDs are lit.

4. Press the "Start Stop" button on the front panel of both CTS units .
5. Press the "results" button on the front panel of both CTS units..
6. Select "Test Summary" on both CTS units.

Verify that there are no "Alarms or Errors" on both CTS units.

TEST CTS Setup

8. Press the "Transmit" button on the front panel.
9. Select "Defect & Anomalies".
10. High light the "Error Type set to" and select "Pattern Bit".
11. Press the "Insert Error" button on the front panel 5 times.
12. Press the "Results" button on the front panel.
13. Select "Test Summary".
14. Verify "Pattern Bit Errors" = 5

CTS (Under Test)

3. Verify "Pattern Bit Errors" = 5
4. Press "Start Stop" and "Clear History" on both units.

140Mb/s External Add/Drop.

Setup CTS (Under Test)

Transmitter	Receiver
TX Rate = **STM-1 Electrical**	RX Rate **= STM-1 Electrical**
TX Clock = **Internal**	Receive Level **= -6dB**
TX Level = **-6dB**	AU Under Test **= 1**
Structure = **140Mb**	Structure **= 140Mb**
Payload **= 140Mb/s External Add**	Payload **= 140Mb/s Framed**
Ext Add Input Level = **Normal (Cross Connect)**	Test Patterns **= PRBS 2^23-1**
TX/RX Setup = **Coupled**	Payload Drop **= Drop 140Mb/s**
	TX/RX Setup **= Coupled**

Setup the TEST CTS

Transmitter	Receiver
TX Rate **= 140Mb/s**	RX Rate = **140 Mb/s**
TX Clock **= Internal**	Receive Level **= Normal (Cross Connect)**
Line Clock Offset **= 0.0ppm**	Payload = **140Mb/s Framed**
Payload **= 140Mb/s framed**	Test Pattern **= PRBS 2^23-1**
Test Pattern = **PRBS 2^23-1**	TX/RX Setup **= Coupled**
TX/RX Setup **= Coupled**	

Verify CTS (Under Test) and TEST CTS "Signal Present and "Pattern Lock" LEDs are lit.

1. Press the "Start Stop" button on the front panel of both CTS units.
2. Press the "results" button on the front panel of both CTS units.
3. Select "Test Summary" on both CTS units.

Verify that there are "No Alarms" and "No Errors" on both CTS units.

1. Disconnect the 75 Ohm cable from the CTS (Under Test) 75 Ohm PDH input.
2. Verify CTS (Under Test) "LOF" led is lit.
3. Verify TEST CTS "LOF" and "ERROR" LEDs are lit.
4. Reconnect the 75 Ohm cable to the CTS (Under Test) 75 Ohm PDH input.
5. Disconnect the 75 Ohm cable from the CTS (Under Test) 75 Ohm STM input.

Verify CTS (Under Test) "LOS" led is lit.

Verify TEST CTS "LOF" and "ERROR" LEDs are lit.

1. Reconnect the 75 Ohm cable to the **CTS (Under Test)** 75 Ohm STM input.
2. Press "Start Stop" and "Clear History" on both units.

Verify CTS (Under Test) and TEST CTS "Signal Present" and "pattern lock" LEDs are lit.

1. Press the "Start Stop" button on the front panel of both CTS units .
2. Press the "results" button on the front panel of both CTS units..
3. Select "Test Summary" on both CTS units.

Verify that there are no "Alarms or Errors" on both CTS units.

TEST CTS Setup

1. Press the "Transmit" button on the front panel.
2. Select "Defect & Anomalies".
3. High light the "Error Type set to" and select "Pattern Bit".
4. Press the "Insert Error" button on the front panel 5 times.
5. Press the "Results" button on the front panel.
6. Select "Test Summary".
7. Verify "Pattern Bit Errors" = 5

CTS (Under Test)

1. Verify "Pattern Bit Errors" = 5
2. Press "Start Stop" and "Clear History" on both units.

2 Mb/s Balanced Transmit Pulse Mask and Amplitude

This test verifies the 120 ohm balanced pulse mask from the 2 Mb/s output of the CTS850.

Equipment Required	TDS784C Digital Scope (item 3) AFTDS adapter probe (item 27) DIN41628L, 120 Ω cable (item 16)
Prerequisites	All previous Physical Layer Tests
Time Required	Approximately fifteen minutes

1. Connect the communications signal analyzer and CTS as shown in Figure 4-15.

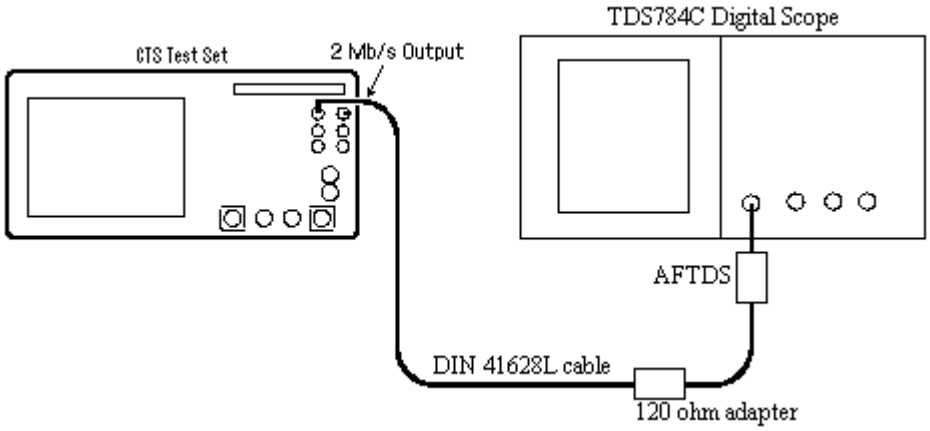


Figure 4-15: 2 Mb/s Pulse Mask Hookup

2. Set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Tx/Rx Settings	Coupled
		Transmit Rate	2 Mb/s HDB3 (Balanced)
		Test Pattern	All Zeros
		Payload Structure	2 Mb/s Unframed

Clock	Internal

3. Set the probe adapter for **120**.

4. Perform the initial setup of the TDS784C with the following steps:

   a. Press the **DISPLAY** button and then press the button to select the **Variable Persistence**.

   b. Using the **SELECT** dial set the Variable Persistence to **2 seconds**.

   c. Press the **TRIGGER** button and then select **Channel 1** by pressing the button.

   d. Press the **MEASURE** button and then select **Masks**.

   e. Under the **Mask Type** menu, select the **ITU-T** menu item.

   f. Select the mask for **E1 Sym pair**.

   j. Press the **AUTOSET** button.

NOTE: *Sometimes, AUTOSET is not effective for mask testing because of trigger thresholds on signals through cable having inter-symbol interference. To minimize visual effects for mask testing, adjust the trigger levels after AUTOSET.*

4. Press the button for the **Timebase Position** menu item and use the horizontal position knob to center the waveform within the mask.

5. On the TDS784C digital scope, press the **CURSOR** button and select the **Horizontal bars**.

6. Move the horizontal bars so that one is at the center of the screen and one is at the top of the signal peak. The difference between these cursors is the V_{pk} value.

2 Mb/s Balanced (20dB) Monitor Receive Level

This test verifies the monitor receive level for the CTS850 Option 38 RECEIVE/ADD input.

Equipment Required	Tributary Signal Converter/Attenuator (item 30), two required 10X (20dB) Attenuator (item 17) 3dB Attenuator (item 19) 120 ohm DIN41628L cable (item 16), two required BNC Male to BNC Male Adapter (item 22)
Prerequisites	All previous Physical Layer Tests
Time Required	Approximately ten minutes

1. Connect the CTS as shown in Figure 4-16.

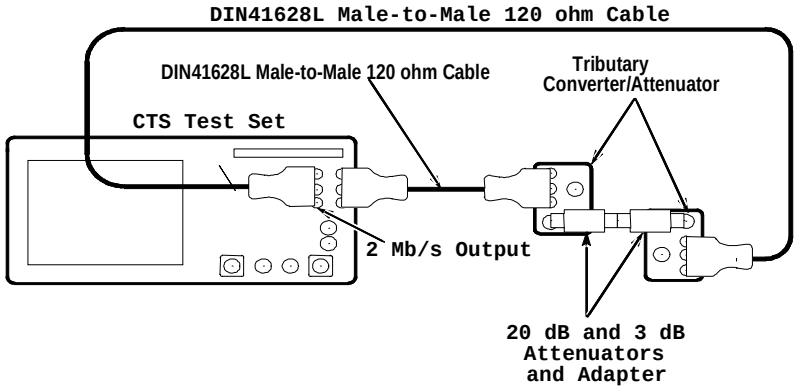


Figure 4-16: 2 Mb/s Balanced (20dB) Monitor Receive Level Hookup

2. Set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TEST SETUPS	TEST CONTROL	Test Duration	USER DEFINED
			Minute
			Rotate knob for 2 m
			DONE
TRANSMIT	TRANSMIT SETTINGS	Tx/Rx Settings	Coupled
		Transmit Rate	2 Mb/s HDB3 (Balanced)
		Test Pattern	PRBS 2^23-1 normal
		Payload Structure	2 Mb/s Unframed
RECEIVE	RECEIVE SETTINGS	Receive Level	Monitor (-20 dB)
RESULTS	MAIN RESULTS	*None*	PDH Anomalies

3. Perform the test with the following steps:

a. Press the **START/STOP** button and verify that the START/STOP light is on.

b. Wait two minutes for the test to complete; the START/STOP light turns off when the test is complete.

c. Verify that there are no errors.

d. Select **PDH Defects**; verify that there are no alarms.

e. Select **Network Defects**; verify that there are no failures.

2 Mb/s Balanced (30dB) Monitor Receive Level

This test verifies the monitor receive level for the CTS850 Option 38 RECEIVE/ADD input.

Equipment Required	Tributary Signal Converter/Attenuator (item 30), two required 10X (20dB) Attenuator (item 17) 10dB Attenuator (item 20) 3dB Attenuator (item 19) 120 ohm DIN41628L cable (item 16), two required BNC Male to BNC Male Adapter (item 22)
Prerequisites	All previous Physical Layer Tests
Time Required	Approximately ten minutes

1. Connect the CTS as shown in Figure 4-17.

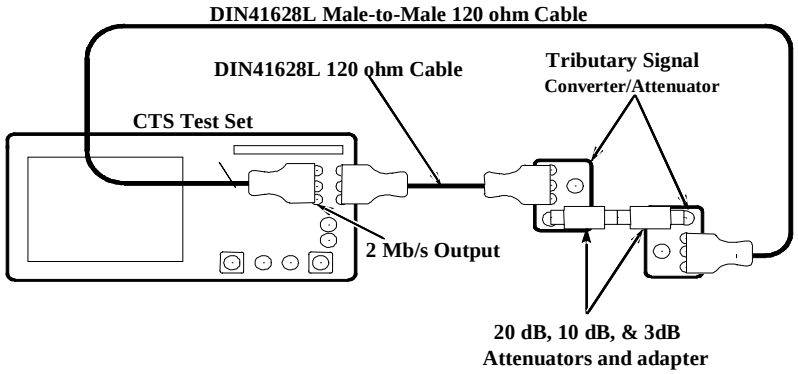


Figure 4-17: 2 Mb/s Balanced (30dB) Monitor Receive Level Hookup

2. Set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TEST SETUPS	TEST CONTROL	Test Duration	USER DEFINED
			Minute
			Rotate knob for 2 m
			DONE
TRANSMIT	TRANSMIT SETTINGS	Tx/Rx Settings	Coupled
		Transmit Rate	2 Mb/s HDB3 (Balanced)
		Test Pattern	PRBS 2^23-1 normal
		Payload Structure	2 Mb/s Unframed
RECEIVE	RECEIVE SETTINGS	Receive Level	Monitor (-30 dB)
RESULTS	MAIN RESULTS	*None*	PDH Anomalies

3. Perform the test with the following steps:

a. Press the **START/STOP** button and verify that the START/STOP light is on.

b. Wait two minutes for the test to complete; the START/STOP light turns off when the test is complete.

c. Verify that there are no errors.

d. Select **PDH Defects**; verify that there are no alarms.

e. Select **Network Defects**; verify that there are no failures.

2 Mb/s Balanced Bridged Receive Level

This test verifies the bridged receive level for the CTS 2 Mb/s input.

Equipment Required	Tributary Signal Converter/Attenuator (item 30), two required 50 Ω BNC cable (item 31) 120 Ω DIN41628L cable (item 16), two required 50 Ω thru-terminator (item 29)
Prerequisites	All previous Physical Layer Tests
Time Required	Approximately ten minutes

1. Connect the CTS as shown in Figure 4-18.

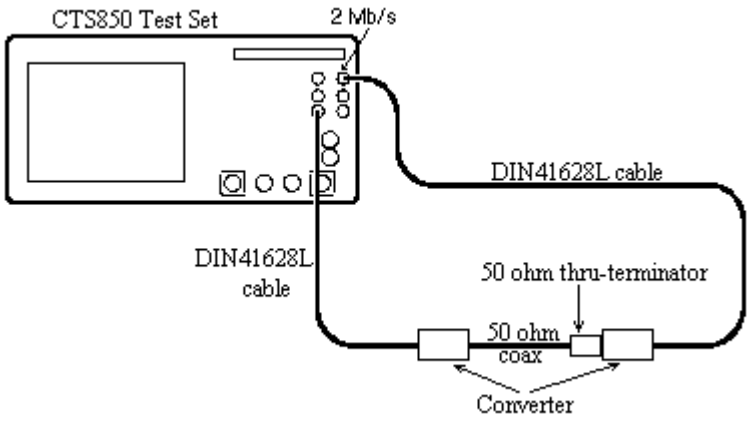


Figure 4-18: 2 Mb/s Bridged Hookup

2. Set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TEST SETUPS	TEST CONTROL	Test Duration	USER DEFINED
			Minute
			Rotate knob for 2 m
			DONE
TRANSMIT	TRANSMIT SETTINGS	Tx/Rx Settings	Coupled
		Transmit Rate	2 Mb/s HDB3 (Balanced)
		Test Pattern	PRBS 2^23-1 normal
		Payload Structure	2 Mb/s Unframed
RECEIVE	RECEIVE SETTINGS	Receive Level	Bridge
RESULTS	MAIN RESULTS	*none*	PDH Anomalies

3. Perform the test with the following steps:

a. Press the **START/STOP** button and verify that the START/STOP light is on.

b. Wait two minutes for the test to complete; the START/STOP light turns off when the test is complete.

c. Verify that there are no errors.

d. Select **PDH Defects**; verify that there are no alarms.

e. Select **Network Defects**; verify that there are no failures.

2 Mb/s Unbalanced Transmit Pulse Mask and Amplitude

This test verifies the 2 Mb/s pulse mask from the CTS850.

Equipment Required	TDS784C Digital Scope (item 3) AMT75 adapter probe (item 28) 75 Ω coaxial cable (item 12)
Prerequisites	All previous Physical Layer Tests
Time Required	Approximately fifteen minutes

1. Connect the communications signal analyzer and CTS as shown in Figure 4-19.

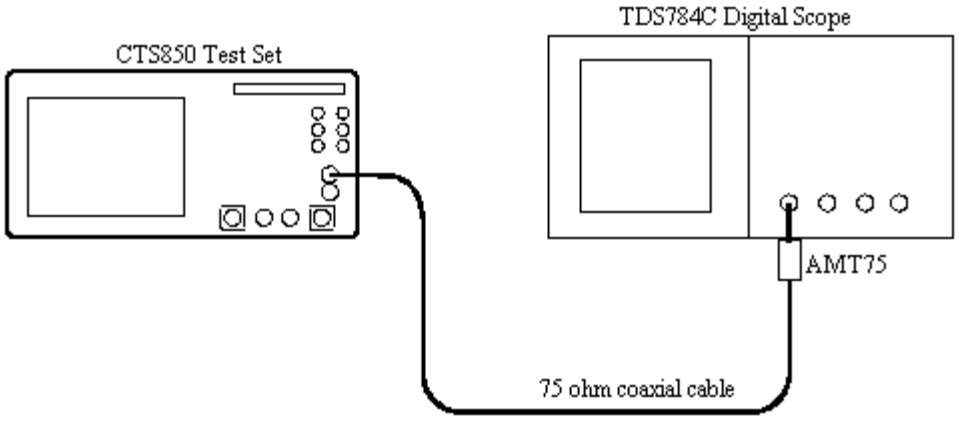


Figure 4-19: 2 Mb/s Pulse Mask Hookup

2. Set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Tx/Rx Settings	Coupled
		Transmit Rate	2 Mb/s HDB3 (Unbalanced)
		Test Pattern	All Zeros
		Payload Structure	2 Mb/s Unframed
RESULTS	MAIN RESULTS	*none*	PDH Anomalies

3. Perform the initial setup of the TDS784C with the following steps:

   a. Press the **DISPLAY** button and then press the button to select the **Variable Persistence**.

   b. Using the **SELECT** dial set the Variable Persistence to **2 seconds**.

   c. Press the **TRIGGER** button and then select **Channel 1** by pressing the button.

   d. Press the **MEASURE** button and then select **Masks**.

   e. Under the **Mask Type** menu, select the **ITU-T** menu item.

   f. Select the mask for **E1 coax**.

   k. Press the **AUTOSET** button.

NOTE: *Sometimes, AUTOSET is not effective for mask testing because of trigger thresholds on signals through cable having inter-symbol interference. To minimize visual effects for mask testing, adjust the trigger levels after AUTOSET.*

4. Press the button for the **Timebase Position** menu item and use the horizontal position knob to center the waveform within the mask.
5. On the TDS784C digital scope, press the **CURSOR** button and select the **Horizontal bars**.
6. Move the horizontal bars so that one is at the center of the screen and one is at the top of the signal peak. The difference between these cursors is the V_{pk} value.

8 Mb/s Unbalanced Transmit Pulse Mask

This test verifies the 8 Mb/s pulse mask from the CTS.

Equipment Required	TDS784C Digital Scope (item 3) AMT75 adapter probe (item 28) 75 Ω coaxial cable (item 12)
Prerequisites	All previous Physical Layer Tests
Time Required	Approximately fifteen minutes

1. Connect the communications signal analyzer and CTS as shown in Figure 4-20.

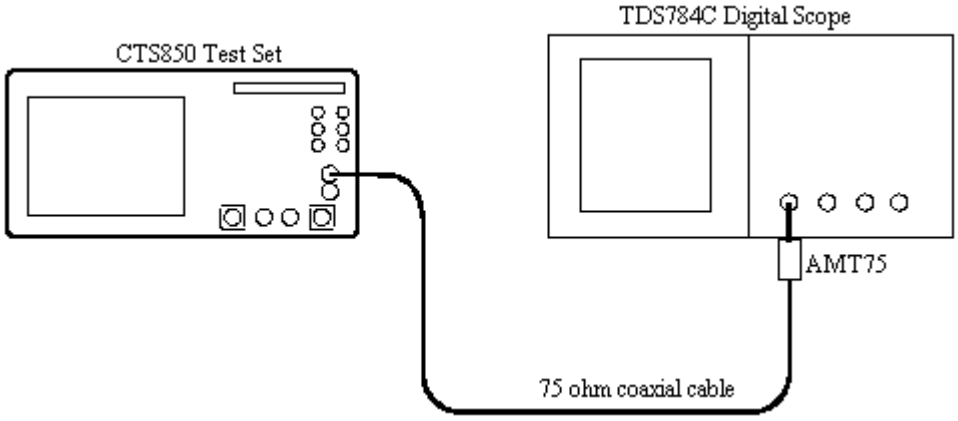


Figure 4-20: 8 Mb/s Pulse Mask Hookup

2. Set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Tx/Rx Settings	Coupled
		Transmit Rate	8 Mb/s HDB3
		Test Pattern	All Zeros
		Payload Structure	8 Mb/s Unframed

3. Perform the initial setup of the TDS784C with the following steps:

   a. Press the **DISPLAY** button and then press the button to select the **Variable Persistence**.

   b. Using the **SELECT** dial set the Variable Persistence to **2 seconds**.

   c. Press the **TRIGGER** button and then select **Channel 1** by pressing the button.

   d. Press the **MEASURE** button and then select **Masks**.

   e. Under the **Mask Type** menu, select the **ITU-T** menu item.

   f. Select the mask for **E2**.

   g. Press the **AUTOSET** button.

NOTE: *Sometimes, AUTOSET is not effective for mask testing because of trigger thresholds on signals through cable having inter-symbol interference. To minimize visual effects for mask testing, adjust the trigger levels after AUTOSET.*

4. Press the button for the **Timebase Position** menu item and use the horizontal position knob to center the waveform within the mask.
5. On the TDS784C digital scope, press the **CURSOR** button and select the **Horizontal bars**.
6. Move the horizontal bars so that one is at the center of the screen and one is at the top of the signal peak. The difference between these cursors is the V_{pk} value.

34 Mb/s Unbalanced Transmit Pulse Mask and Amplitude

This test verifies the 34 Mb/s pulse mask from the CTS.

Equipment Required	TDS784C Digital Scope (item 3) AMT75 adapter probe (item 28) 75 Ω coaxial cable (item 12)
Prerequisites	All previous Physical Layer Tests
Time Required	Approximately fifteen minutes

1. Connect the communications signal analyzer and CTS as shown in Figure 4-21.

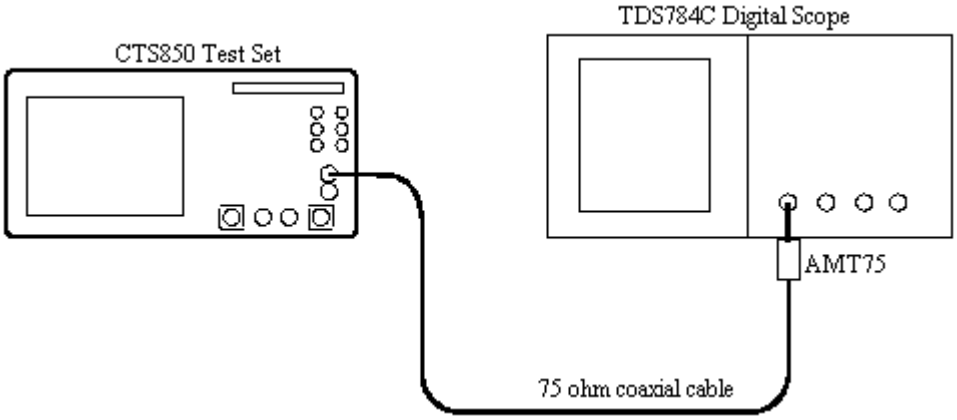


Figure 4-21: 34 Mb/s Pulse Mask Hookup

2. Set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Tx/Rx Settings	Coupled
		Transmit Rate	34 Mb/s HDB3
		Test Pattern	All Zeros
		Payload Structure	34 Mb/s Unframed

3. Perform the initial setup of the TDS784C with the following steps:

   a. Press the **DISPLAY** button and then press the button to select the **Variable Persistence**.

   b. Using the **SELECT** dial set the Variable Persistence to **2 seconds**.

   c. Press the **TRIGGER** button and then select **Channel 1** by pressing the button.

   d. Press the **MEASURE** button and then select **Masks**.

   e. Under the **Mask Type** menu, select the **ITU-T** menu item.

   f. Select the mask for **E3**.

   g. Press the **AUTOSET** button.

NOTE: *Sometimes, AUTOSET is not effective for mask testing because of trigger thresholds on signals through cable having inter-symbol interference. To minimize visual effects for mask testing, adjust the trigger levels after AUTOSET.*

4. Press the button for the **Timebase Position** menu item and use the horizontal position knob to center the waveform within the mask.
5. On the TDS784C digital scope, press the **CURSOR** button and select the **Horizontal bars**.
6. Move the horizontal bars so that one is at the center of the screen and one is at the top of the signal peak. The difference between these cursors is the V_{pk} value.

Option 55 Only

45 Mb/s Unbalanced Transmit Pulse Mask & Amplitude (-6dB)

This test verifies the 45 Mb/s pulse mask from the CTS.

Equipment Required	TDS784C Digital Scope (item 3) AMT75 adapter probe (item 28) 75 Ω coaxial cable (item 12)
Prerequisites	All previous Physical Layer Tests
Time Required	Approximately fifteen minutes

1. Connect the communications signal analyzer and CTS as shown in Figure 4-22.

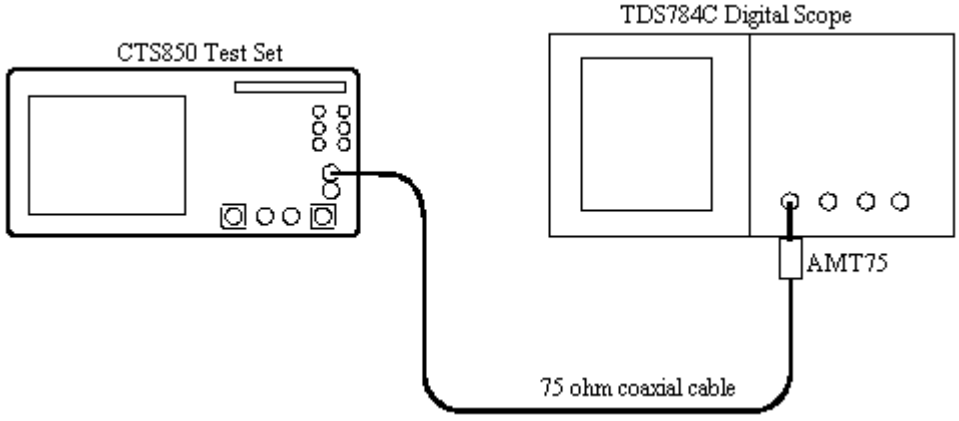


Figure 4-22: 45 Mb/s Pulse Mask Hookup (-6dB)

2. Set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Tx/Rx Settings	Coupled
		Transmit Rate	45 Mb/s HDB3
		Transmit Level	-6 dB
		Test Pattern	All Zeros
		Payload Structure	45 Mb/s Unframed

3. Perform the initial setup of the TDS784C with the following steps:

   a. Press the **DISPLAY** button and then press the button to select the **Variable Persistence**.

   b. Using the **SELECT** dial set the Variable Persistence to **2 seconds**.

   c. Press the **TRIGGER** button and then select **Channel 1** by pressing the button.

   d. Press the **MEASURE** button and then select **Masks**.

   e. Under the **Mask Type** menu, select the **T1.102** menu item.

   f. Select the mask for **DS3**.

   g. Press the **AUTOSET** button.

NOTE: *Sometimes, AUTOSET is not effective for mask testing because of trigger thresholds on signals through cable having inter-symbol interference. To minimize visual effects for mask testing, adjust the trigger levels after AUTOSET.*

4. Press the button for the **Timebase Position** menu item and use the horizontal position knob to center the waveform within the mask.

5. On the TDS784C digital scope, press the **CURSOR** button and select the **Horizontal bars**.

6. Move the horizontal bars so that one is at the center of the screen and one is at the top of the signal peak. The difference between these cursors is the V_{pk} value.

Option 55 Only

45 Mb/s Unbalanced Transmit Pulse Mask and Amplitude (0dB)

This test verifies the 45 Mb/s pulse mask from the CTS.

Equipment Required	TDS784C Digital Scope (item 3) AMT75 adapter probe (item 28) 450ft coax cable (item 11) BNC female-to-female adapter (item 13)
Prerequisites	All previous Physical Layer Tests
Time Required	Approximately fifteen minutes

1. Connect the communications signal analyzer and CTS as shown in Figure 4-23.

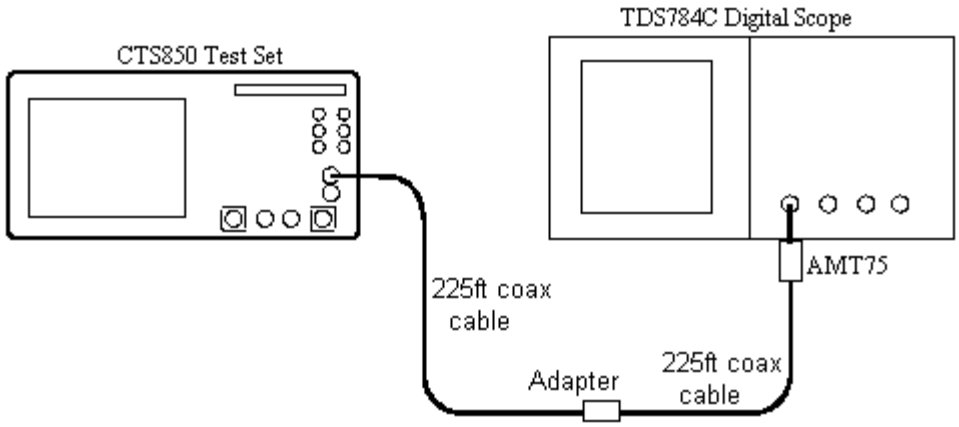


Figure 4-23: 45 Mb/s Pulse Mask Hookup (0dB)

2. Set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Tx/Rx Settings	Coupled
		Transmit Rate	45 Mb/s HDB3
		Transmit Level	0 dB
		Test Pattern	All Zeros
		Payload Structure	45 Mb/s Unframed

3. Perform the initial setup of the TDS784C with the following steps:

   a. Press the **DISPLAY** button and then press the button to select the **Variable Persistence**.

   b. Using the **SELECT** dial set the Variable Persistence to **2 seconds**.

   c. Press the **TRIGGER** button and then select **Channel 1** by pressing the button.

   d. Press the **MEASURE** button and then select **Masks**.

   e. Under the **Mask Type** menu, select the **T1.102** menu item.

   f. Select the mask for **DS3**.

   g. Press the **AUTOSET** button.

NOTE: *Sometimes, AUTOSET is not effective for mask testing because of trigger thresholds on signals through cable having inter-symbol interference. To minimize visual effects for mask testing, adjust the trigger levels after AUTOSET.*

4. Press the button for the **Timebase Position** menu item and use the horizontal position knob to center the waveform within the mask.

5. On the TDS784C digital scope, press the **CURSOR** button and select the **Horizontal bars**.

6. Move the horizontal bars so that one is at the center of the screen and one is at the top of the signal peak. The difference between these cursors is the V_{pk} value.

140 Mb/s Unbalanced Transmit Pulse Mask and Amplitude

This test verifies the 140 Mb/s pulse mask from the CTS.

Equipment Required	TDS784C Digital Scope (item 3) AMT75 adapter probe (item 28) 75 Ω coaxial cable (item 12)
Prerequisites	All previous Physical Layer Tests
Time Required	Approximately fifteen minutes

1. Connect the communications signal analyzer and CTS as shown in Figure 4-24.

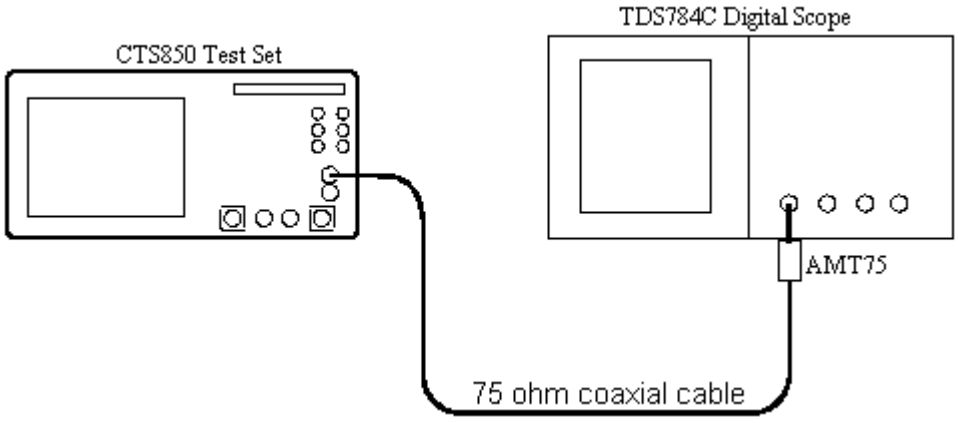


Figure 4-24: 140 Mb/s Pulse Mask Hookup

2. Set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Tx/Rx Settings	Coupled
		Transmit Rate	140 Mb/s
		Test Pattern	All Ones
		Payload Structure	140 Mb/s Unframed

3. Perform the initial setup of the TDS784C with the following steps:

   a. Press the **DISPLAY** button and then press the button to select the **Variable Persistence**.

   b. Using the **SELECT** dial set the Variable Persistence to **2 seconds**.

   c. Press the **TRIGGER** button and then select **Channel 1** by pressing the button.

   d. Press the **MEASURE** button and then select **Masks**.

   e. Under the **Mask Type** menu, select the **ITU-T** menu item.

   f. Select the mask for **E4 Binary 1**.

   l. Press the **AUTOSET** button.

NOTE: *Sometimes, AUTOSET is not effective for mask testing because of trigger thresholds on signals through cable having inter-symbol interference. To minimize visual effects for mask testing, adjust the trigger levels after AUTOSET.*

4. Press the button for the **Timebase Position** menu item and use the vertical position knob and the horizontal position knob to center the waveform within the mask.

5. On the TDS784C digital scope, press the **CURSOR** button and select the **Horizontal bars**.

6. Move the horizontal bars so that one is at the center of the screen and one is at the top of the signal peak. The difference between these cursors is the V_{pp} value.

7. Change the **Transmit Pattern** on the CTS to **All Zeros**.

8. Change the setup of the TDS784C with the following steps:

   a. Press the **MEASURE** button and then select **Masks**.

   b. Under the **Mask Type** menu, select the **ITU-T** menu item.

   c. Select the mask for **E4 Binary 0**.

   d. Press the **AUTOSET** button.

NOTE: *Sometimes, AUTOSET is not effective for mask testing because of trigger thresholds on signals through cable having inter-symbol interference. To minimize visual effects for mask testing, adjust the trigger levels after AUTOSET.*

9. Press the button for the **Timebase Position** menu item and use the vertical position knob and the horizontal position knob to center the waveform within the mask.
10. On the TDS784C digital scope, press the **CURSOR** button and select the **Horizontal bars**.
11. Move the horizontal bars so that one is at the center of the screen and one is at the top of the signal peak. The difference between these cursors is the V_{pp} value.

2 Mb/s Unbalanced (20dB) Monitor Receive Level

This test verifies the 2 Mb/s unbalanced monitor (20dB) receive level of the CTS.

Equipment Required	10X (20dB) Attenuator (item 17) 3dB Attenuator (item 19) 75 Ω coax cable (item 12)
Prerequisites	All previous Physical Layer Tests
Time Required	Approximately ten minutes

1. Connect the CTS as shown in Figure 4-25.

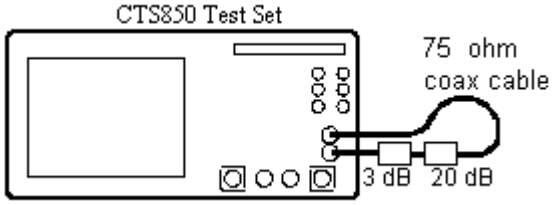


Figure 4-25: 2 Mb/s Unbalanced (20dB) Monitor Receive Level Hookup

2. Set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Tx/Rx Settings	Coupled
		Transmit Rate	2 Mb/s HDB3 (Unbalanced)
		Test Pattern	PRBS 2^23-1 normal
		Payload Structure	2 Mb/s Unframed
RECEIVE	RECEIVE SETTINGS	Receive Level	Monitor (-20 dB)
RESULTS	MAIN RESULTS	*none*	PDH Anomalies

3. Press the **START/STOP** button and verify that the START/STOP light is on.

4. Verify that there are no bit errors or bipolar violations for a measurement period of at least 30 seconds.

2 Mb/s Unbalanced (30dB) Monitor Receive Level

This test verifies the 2 Mb/s unbalanced monitor (30dB) receive level of CTS.

Equipment Required	10X (20dB) Attenuator (item 17) 10 dB Attenuator (item 20) 3dB Attenuator (item 19) 75 ohm coaxial cable (item 12)
Prerequisites	All previous Physical Layer Tests
Time Required	Approximately ten minutes

1. Connect the CTS as shown in Figure 4-26.

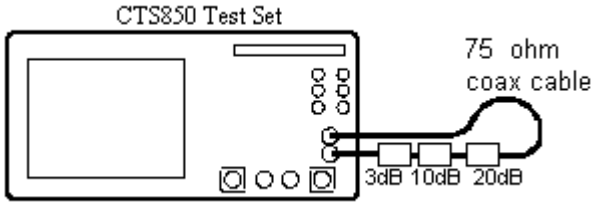


Figure 4-26: 2 Mb/s Unbalanced (30dB) Monitor Receive Level Hookup

2. Set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Tx/Rx Settings	Coupled
		Transmit Rate	2 Mb/s HDB3 (Unbalanced)
		Test Pattern	PRBS 2^23-1 normal
		Payload Structure	2 Mb/s Unframed
RECEIVE	RECEIVE SETTINGS	Receive Level	Monitor (-30 dB)
RESULTS	MAIN RESULTS	*none*	PDH Anomalies

3. Press the **START/STOP** button and verify that the START/STOP light is on.

4. Verify that there are no bit errors or bipolar violations for a measurement period of at least 30 seconds.

8 Mb/s Unbalanced Monitor Receive Level

This test verifies the 8 Mb/s unbalanced monitor receive level of the CTS.

Equipment Required	10X (20dB) Attenuator (item 17) 3dB Attenuator (item 19) 75 Ω coax cable (item 12)
Prerequisites	All previous Physical Layer Tests
Time Required	Approximately ten minutes

1. Connect the CTS as shown in Figure 4-27.

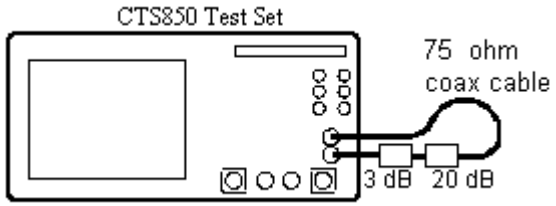


Figure 4-27: 8 Mb/s Unbalanced Monitor Receive Level Hookup

2. Set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Tx/Rx Settings	Coupled
		Transmit Rate	8 Mb/s HDB3
		Test Pattern	PRBS 2^23-1 normal
		Payload Structure	8 Mb/s Unframed
RECEIVE	RECEIVE SETTINGS	Receive Level	Monitor
RESULTS	MAIN RESULTS	*none*	PDH Anomalies

3. Press the **START/STOP** button and verify that the START/STOP light is on.

4. Verify that there are no bit errors or bipolar violations for a measurement period of at least 30 seconds.

34 Mb/s Unbalanced (20dB) Monitor Receive Level

This test verifies the 34 Mb/s unbalanced monitor (20dB) receive level of the CTS.

Equipment Required	10X (20dB) Attenuator (item 17) 3dB Attenuator (item 19) 75 Ω coax cable (item 12)
Prerequisites	All previous Physical Layer Tests
Time Required	Approximately ten minutes

1. Connect the CTS as shown in Figure 4-28.

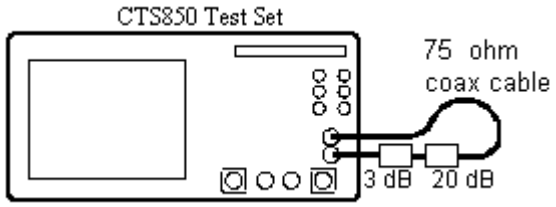


Figure 4-28: 34 Mb/s Unbalanced (20dB) Monitor Receive Level Hookup

2. Set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Tx/Rx Settings	Coupled
		Transmit Rate	34 Mb/s HDB3
		Test Pattern	PRBS 2^23-1 normal
		Payload Structure	34 Mb/s Unframed
RECEIVE	RECEIVE SETTINGS	Receive Level	Monitor (-20 dB)
RESULTS	MAIN RESULTS	*none*	PDH Anomalies

3. Press the **START/STOP** button and verify that the START/STOP light is on.

4. Verify that there are no bit errors or bipolar violations for a measurement period of at least 30 seconds.

34 Mb/s Unbalanced (30dB) Monitor Receive Level

This test verifies the 34 Mb/s unbalanced monitor receive level of the CTS.

Equipment Required	10 dB Attenuator (item 20) 10X (20dB) Attenuator (item 17) 3dB Attenuator (item 19) 75 Ω coax cable (item 12)
Prerequisites	All previous Physical Layer Tests
Time Required	Approximately ten minutes

1. Connect the CTS as shown in Figure 4-29.

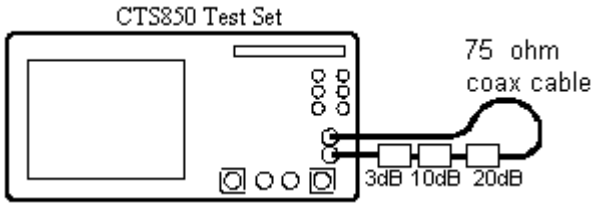


Figure 4-29: 34 Mb/s Unbalanced (30dB) Monitor Receive Level Hookup

2. Set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Tx/Rx Settings	Coupled
		Transmit Rate	34 Mb/s HDB3
		Test Pattern	PRBS 2^23-1 normal
		Payload Structure	34 Mb/s Unframed
RECEIVE	RECEIVE SETTINGS	Receive Level	Monitor (-30 dB)
RESULTS	MAIN RESULTS	*none*	PDH Anomalies

3. Press the **START/STOP** button and verify that the START/STOP light is on.

4. Verify that there are no bit errors or bipolar violations for a measurement period of at least 30 seconds.

Option 55 Only

45 Mb/s Unbalanced (20dB) Monitor Receive Level

This test verifies the 45 Mb/s unbalanced monitor (20dB) receive level of the CTS.

Equipment Required	10X (20dB) Attenuator (item 17) 3dB Attenuator (item 19) 75 Ω coax cable (item 12)
Prerequisites	All previous Physical Layer Tests
Time Required	Approximately ten minutes

1. Connect the CTS as shown in Figure 4-30.

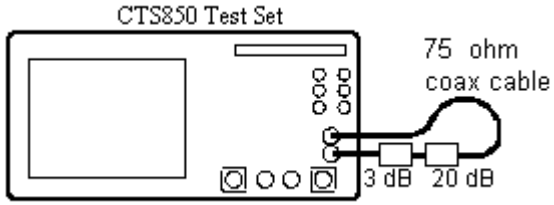


Figure 4-30: 45 Mb/s Unbalanced (20dB) Monitor Receive Level Hookup

2. Set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Tx/Rx Settings	Coupled
		Transmit Rate	45 Mb/s HDB3
		Transmit Level	0 dB
		Test Pattern	PRBS 2^23-1 normal
		Payload Structure	45 Mb/s Unframed
RECEIVE	RECEIVE SETTINGS	Receive Level	Monitor (-20 dB)

RESULTS	MAIN RESULTS	*none*	PDH Anomalies

3. Press the **START/STOP** button and verify that the START/STOP light is on.
4. Verify that there are no bit errors or bipolar violations for a measurement period of at least 30 seconds.

140 Mb/s Unbalanced (20dB) Monitor Receive Level

This test verifies the 140 Mb/s unbalanced monitor receive level for the CTS.

Equipment Required	75 Ω coax cable (item 12) 10X (20dB) Attenuator (item 17) 3dB Attenuator (item 19)
Prerequisites	All previous Physical Layer Tests
Time Required	Approximately ten minutes

1. Connect the CTS as shown in Figure 4-31.

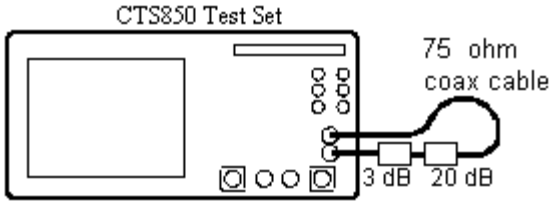


Figure 4-31: 140 Mb/s Unbalanced (20dB) Monitor Receive Level Hookup

2. Set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Tx/Rx Settings	Coupled
		Transmit Rate	140 Mb/s
		Test Pattern	PRBS 2^23-1 normal
		Payload Structure	140 Mb/s Unframed
RECEIVE	RECEIVE SETTINGS	Receive Level	Monitor (-20 dB)
RESULTS	MAIN RESULTS	*none*	PDH Anomalies

3. Press the **START/STOP** button: verify that the START/STOP light is on.

4. Verify that there are no bit errors or bipolar violations for a measurement period of at least 30 seconds.

140 Mb/s Unbalanced (30dB) Monitor Receive Level

This test verifies the 140 Mb/s monitor receive level for the CTS.

Equipment Required	75 Ω coax cable (item 12) 10X (20dB) Attenuator (item 17) 3dB Attenuator (item 19) 6dB Attenuator (item 18)
Prerequisites	All previous Physical Layer Tests
Time Required	Approximately ten minutes

1. Connect the CTS as shown in Figure 4-32.

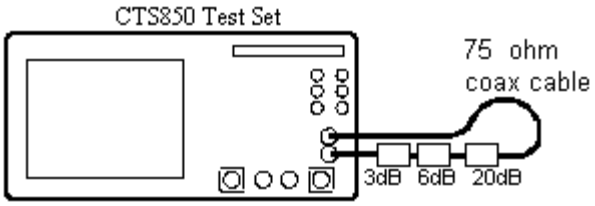


Figure 4-32: 140 Mb/s Unbalanced (30dB) Monitor Receive Level Hookup

2. Set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Tx/Rx Settings	Coupled
		Transmit Rate	140 Mb/s
		Test Pattern	PRBS 2^23-1 normal
		Payload Structure	140 Mb/s Unframed
RECEIVE	RECEIVE SETTINGS	Receive Level	Monitor (-30 dB)
RESULTS	MAIN RESULTS	*none*	PDH Anomalies

3. Press the **START/STOP** button: verify that the START/STOP light is on.

4. Verify that there are no bit errors or bipolar violations for a measurement period of at least 30 seconds.

2 Mb/s Balanced Normal Cable Tolerance

This test verifies the 2 Mb/s normal cable tolerance of the CTS.

Equipment Required	2 Mb/s Signal Source (item 4) 120 Ω DIN41628L cable (item 16)
Prerequisites	All previous Physical Layer Tests
Time Required	Approximately ten minutes

1. Connect the CTS as shown in Figure 4-33.

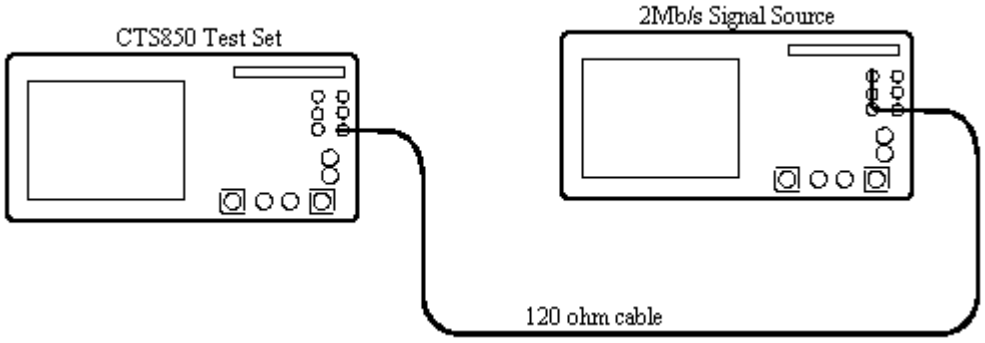


Figure 4-33: 2 Mb/s Balanced Normal Cable Tolerance Hookup

2. Perform the initial setup of the 2 Mb/s Signal Source with the following steps:

   a. Set the 2 Mb/s Signal Source to output a 2 Mb/s HDB3 balanced, PRBS2^23-1 normal unframed signal.

3. Set up the CTS (under test) with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
RECEIVE	RECEIVE SETTINGS	Receive Rate	2 Mb/s HDB3 Balanced
		Receive Level	Normal
		Test Pattern	PRBS 2^23-1 normal
		Payload Structure	2 Mb/s Unframed
RESULTS	MAIN RESULTS	*none*	PDH Anomalies

4. Press the **START/STOP** button and verify that the START/STOP light is on.

5. Verify that there are no bit errors or bipolar violations for a measurement period of at least 30 seconds.

2 Mb/s Unbalanced Cable Equalization

This test verifies the 2 Mb/s cable equalization of the CTS.

Equipment Required	2 Mb/s Signal Source (item 5) 656 ft (200 m) length of 75 Ω Reference Cable (items 10, 11, and 23 connected in series) Adapter, BNC-f to BNC-f (item 13), three required
Prerequisites	All previous Physical Layer Tests
Time Required	Approximately ten minutes

1. Connect the CTS as shown in Figure 4-34.

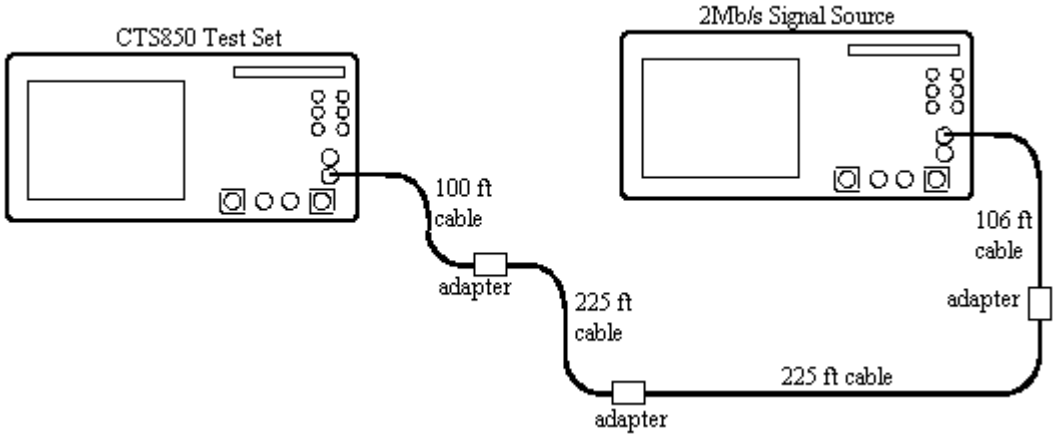


Figure 4-34: 2 Mb/s Cable Equalization Hookup

2. Perform the initial setup of the 2 Mb/s Signal Source with the following steps:

a. Set the 2 Mb/s Signal Source to output a 2 Mb/s HDB3 balanced, PRBS2^23-1 normal unframed signal.

3. Set up the CTS (under test) with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
RECEIVE	RECEIVE SETTINGS	Receive Rate	2 Mb/s HDB3 Unbalanced
		Receive Level	Normal
		Test Pattern	PRBS 2^23-1 normal
		Payload Structure	2 Mb/s Unframed
RESULTS	MAIN RESULTS	*none*	PDH Anomalies

4. Verify that there are no bit errors or bipolar violations for a measurement period of at least 30 seconds.

8 Mb/s Unbalanced Cable Equalization

This test verifies the 8 Mb/s cable equalization of the CTS.

Equipment Required	8 Mb/s Signal Source (item 5) 656 ft (200 m) length of 75 Ω Reference Cable (items 10, 11, and 23 connected in series) Adapter, BNC-f to BNC-f (item 13), three required
Prerequisites	All previous Physical Layer Tests
Time Required	Approximately ten minutes

1. Connect the CTS as shown in Figure 4-35.

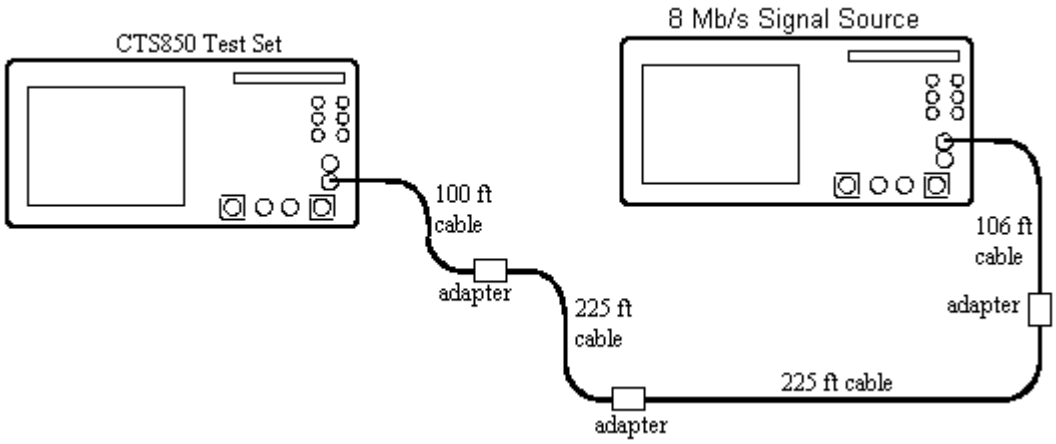


Figure 4-35: 8 Mb/s Cable Equalization Hookup

2. Perform the initial setup of the 8 Mb/s Signal Source with the following steps:

   a. Set the 8 Mb/s Signal Source to output a 8 Mb/s HDB3 balanced, PRBS2^23-1 normal unframed signal.

3. Set up the CTS (under test) with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
RECEIVE	RECEIVE SETTINGS	Receive Rate	8 Mb/s HDB3 Unbalanced
		Receive Level	Normal
		Test Pattern	PRBS 2^23-1 normal
		Payload Structure	8 Mb/s Unframed
RESULTS	MAIN RESULTS	*none*	PDH Anomalies

4. Verify that there are no bit errors or bipolar violations for a measurement period of at least 30 seconds.

34 Mb/s Cable Equalization

This test verifies the 34 Mb/s cable equalization for the CTS.

Equipment Required	34 Mb/s Signal Source (item 5) 656 ft (200 m) length of 75 Ω Reference Cable (items 10, 11, and 23 connected in series) Adapter, BNC-f to BNC-f (item 13), three required
Prerequisites	All previous Physical Layer Tests
Time Required	Approximately ten minutes

1. Connect the CTS as shown in Figure 4-36.

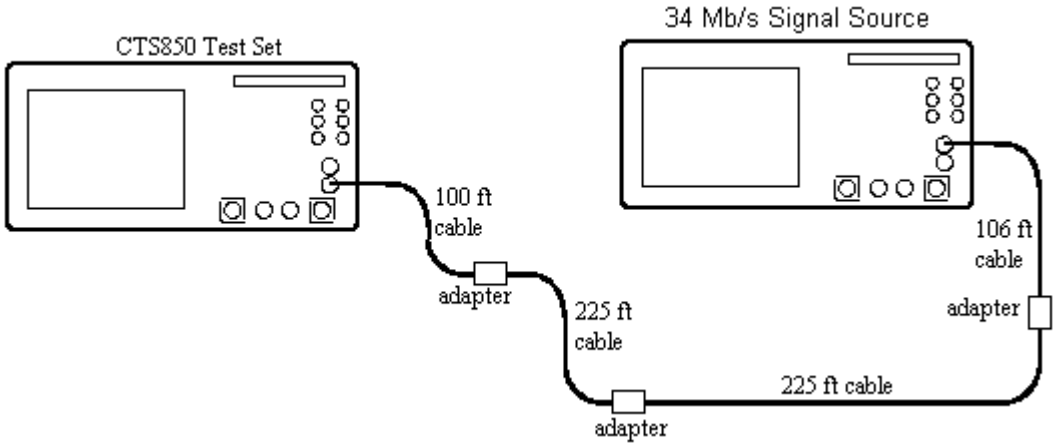


Figure 4-36: 34 Mb/s Cable Equalization Hookup

2. Set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Tx/Rx Settings	Coupled
		Transmit Rate	34 Mb/s HDB3
		Test Pattern	PRBS 2^23-1 normal
		Payload Structure	34 Mb/s Unframed
RECEIVE	RECEIVE SETTINGS	Receive Level	Normal
RESULTS	MAIN RESULTS	*none*	PDH Anomalies

3. Verify that there are no pattern bit errors or code violations for a measurement period of at least 30 seconds.

Option 55 Only

45 Mb/s Cable Equalization

This test verifies the 45 Mb/s cable equalization for the CTS.

Equipment Required	45 Mb/s Signal Source (item 5) 556 ft length of 75 Ω Reference Cable (items 11 and 23 connected in series) Adapter, BNC-f to BNC-f (item 13), two required
Prerequisites	All previous Physical Layer Tests
Time Required	Approximately ten minutes

1. Connect the CTS as shown in Figure 4-37.

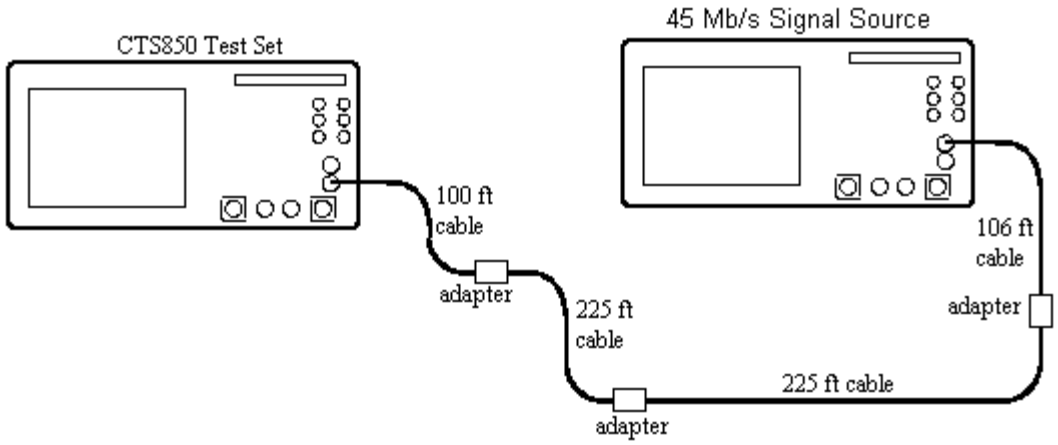


Figure 4-37: 45 Mb/s Cable Equalization Hookup

2. Set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Tx/Rx Settings	Coupled
		Transmit Rate	34 Mb/s HDB3
		Test Pattern	PRBS 2^23-1 normal
		Payload Structure	34 Mb/s Unframed
RECEIVE	RECEIVE SETTINGS	Receive Level	Normal
RESULTS	MAIN RESULTS	*none*	PDH Anomalies

3. Verify that there are no pattern bit errors or code violations for a measurement period of at least 30 seconds.

140 Mb/s Cable Equalization

This test verifies the 140 Mb/s cable equalization for the CTS.

Equipment Required	140 Mb/s Signal Source (item 5) 656 ft (200 m) length of 75 Ω Reference Cable (items 10, 11, and 23 connected in series) Adapter, BNC-f to BNC-f (item 13), three required
Prerequisites	All prerequisites listed on page –1 All previous Physical Layer Tests
Time Required	Approximately ten minutes

1. Connect the CTS as shown in Figure 4-38.

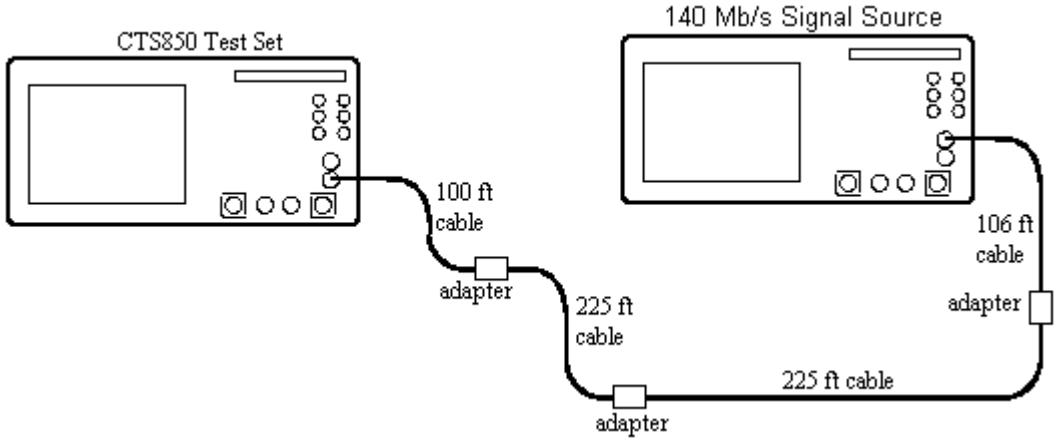


Figure 4-38: 140 Mb/s Cable Equalization Hookup

2. Set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Tx/Rx Settings	Coupled
		Transmit Rate	140 Mb/s
		Test Pattern	PRBS 2^23-1 normal
		Payload Structure	140 Mb/s Unframed
RECEIVE	RECEIVE SETTINGS	Receive Level	Normal
RESULTS	MAIN RESULTS	*none*	PDH Anomalies

3. Verify that there are no pattern bit errors or code violation errored seconds for a measurement period of at least 30 seconds.

This completes the Option 38 (and Option 55) Performance Verification Procedure.

Option 14 - Jitter Performance Verification

Low-Frequency Jitter Tests

Perform the following setup to prepare for the Low–Frequency Jitter Tests.

Equipment Required	75 Ohm BNC coaxial cable, two required (item 12) Optical fiber cable (item 8)
Prerequisites	All previous Physical Layer Tests
Time Required	Approximately 30 minutes

1. Connect the CTS inputs and outputs in a loop–back configuration as shown in Figure 4-39.

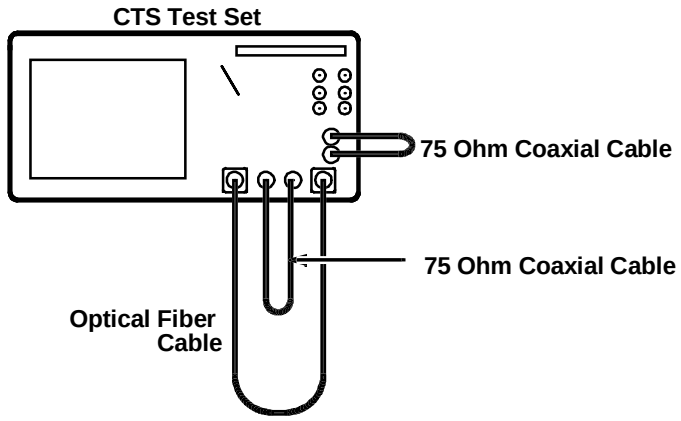


Figure 4-39: Low–Frequency Jitter Test Hookup

2. Perform the initial CTS setup with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Tx/Rx Settings	Coupled
TRANSMIT	JITTER & WANDER	Jitter/Wander Generation	On
		Jitter Output	Line
TEST SETUPS	TEST CONTROL	Test Duration	USER DEFINED
			Second

3. Rotate the knob to set the Test Duration to 30 seconds, and then press **Done**.

NOTE: *In the next steps, you will repeat a jitter measurement for several jitter frequencies and transmit/receive rates. The basic process is described once. Table 4-4 describes the specific conditions for each test. You will repeat the process for each row in Table 4-4.*

4. For each row in Table 4-4, setup the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TRANSMIT	TRANSMIT SETTINGS	Transmit Rate	*as specified in column 1 of Table 4-4**
		Jitter Amplitude	*as specified in column 2 of Table 4-4 **
RECEIVE	JITTER & WANDER	Jitter Range	*as specified in column 3 of Table 4-4*
		Jitter Filter	*as specified in column 4 of Table 4-4*
		Fullband Highpass	*as specified in column 5 of Table 4-4*
TRANSMIT	JITTER & WANDER	Jitter Frequency	*as specified in column 6 of Table 4-4*
RESULTS			Jitter/Wander

*** If the specified value is not one of the available menu choices, choose USER DEFINED, set the value with the knob, and then press DONE.**

5. Press the **START/STOP** button, and verify that the START/STOP light is on.

6. Wait 30 seconds for the test to complete.

7. Verify that the current peak–to–peak jitter measurement is within the limits specified in column 7 of Table 4-4 (inclusive).

8. Repeat steps 4 through 7 for each row in Table 4-4.

Table 4-4. Low–Frequency Jitter Tests

Transmit Rate	Jitter Amplitude	Jitter Range	Jitter Filter	Fullband Highpass	Jitter Frequency	Test Limits
2 Mb/s (Unbalanced)	200 UI	Extended	Fullband	1 Hz	15 Hz	189.29 to 209.82 UI
34 Mb/s	200 UI	Extended	Fullband	1 Hz	15 Hz	189.29 to 209.82 UI
140 Mb/s	200 UI	Extended	Fullband	1 Hz	15 Hz	189.29 to 209.82 UI
STM–0E	200 UI	Extended	Fullband	1 Hz	15 Hz	189.29 to 209.82 UI
STM–1E	200 UI	Extended	Fullband	1 Hz	15 Hz	189.29 to 209.82 UI
STM–4	200 UI	Extended	Fullband	1 Hz	15 Hz	188.79 to 210.32 UI
2 Mb/s (Unbalanced)	15.75 UI	Extended	Fullband	10 Hz	150 Hz	14.82 to 16.61 UI
34 Mb/s	15.75 UI	Extended	Fullband	10 Hz	150 Hz	14.82 to 16.61 UI
140 Mb/s	15.75 UI	Extended	Fullband	10 Hz	150 Hz	14.82 to 16.61 UI
STM–0E	15.75 UI	Extended	Fullband	10 Hz	150 Hz	14.82 to 16.61 UI
STM–1E	15.75 UI	Extended	Fullband	10 Hz	150 Hz	14.82 to 16.61 UI
STM–4	15.75 UI	Extended	Fullband	10 Hz	150 Hz	14.67 to 16.76 UI
45Mb/s *(Option 55 only)*	200 UI	Extended	Fullband	1 Hz	15 Hz	189.29 to 209.82 UI
45Mb/s *(Option 55 only)*	15.75 UI	Extended	Fullband	10 Hz	150 Hz	14.82 to 16.61 UI

High-Amplitude Jitter Tests

Perform the following setup to prepare for the High–Amplitude Jitter Tests.

Equipment Required	Spectrum analyzer (item 7) 75 Ohm BNC coaxial cable, three required (item 12) Optical fiber cable (item 8) 75 Ohm to 50 Ohm impedance converter (item 32) N–to–BNC adapter (item 14)
Prerequisites	None
Time Required	Approximately 90 minutes

1. Perform the initial CTS setup with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Tx/Rx Settings	Coupled
TEST SETUPS	TEST CONTROL	Test Duration	USER DEFINED
			Second

2. Rotate the knob to set the Test Duration to 30 seconds, and then press **Done**.

CAUTION: *To prevent damage to the spectrum analyzer, follow the next step carefully before completing the instrument hookup.*

3. Perform the initial setup of the spectrum analyzer with the following steps:
   a. Set the reference level to **0 dBm**.
   b. Set the vertical scale factor to **10 dB/division**.
   c. Set the sweep to **free run**.
   d. Set the sweep to **auto** (or **coupled**).

4. Connect the CTS inputs and outputs in a loop–back configuration. Also, connect the rear–panel jitter clock output (J/CLK) to the spectrum analyzer RF input as shown in Figure 4-40.

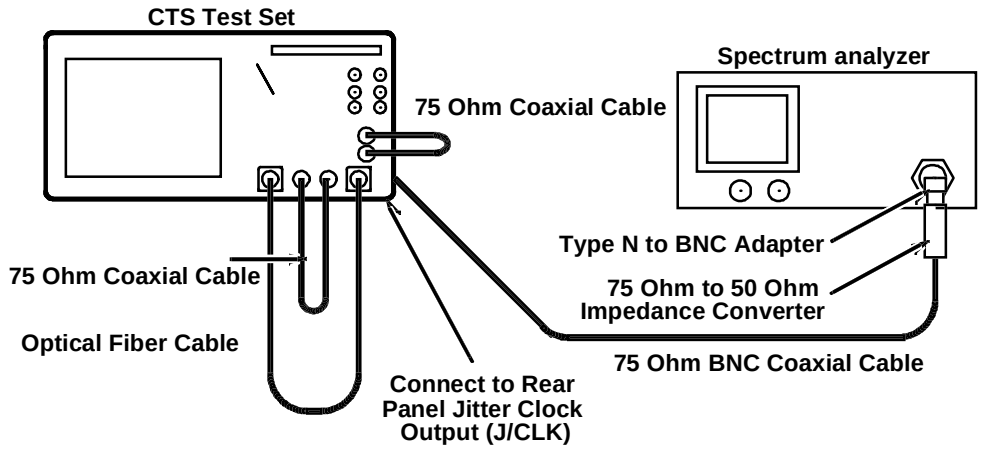


Figure 4-40: High-Amplitude Jitter Test Hookup

NOTE: *In the next steps, you will repeat a jitter measurement for several jitter frequencies and transmit/receive rates. The basic process is described once. The three tables that follow describe the specific conditions for each test. You will repeat the process for each row in the tables.*

5. For each row in Table 4-5, set up the spectrum analyzer as follows:

   a. Set the span (total over 10 divisions) to the value in column 3 of Table 4-5.

   b. Set both the resolution bandwidth and video bandwidth to the value in column 4 of Table 4-5.

   c. Set the center frequency to the value in column 5 of Table 4-5.

Table 4-5: High-Amplitude Spectrum Analyzer Setups

COLUMN 1	*COLUMN 2*	*COLUMN 3*	*COLUMN 4*	*COLUMN 5*
Transmit/Clock Rate	**Jitter Frequency**	**Ten–Division Span**	**Resolution Bandwidth and Video Bandwidth**	**Center Frequency**
2 Mb/s (Unbalanced)	2.5 KHz	10 KHz	300 Hz	2.048 MHz
2 Mb/s (Unbalanced)	1.8 KHz	5 KHz	300 Hz	2.048 MHz
2 Mb/s (Unbalanced)	6.4 KHz	20 KHz	1 KHz	2.048 MHz
34 Mb/s	2.5 KHz	10 KHz	300 Hz	34.368 MHz
34 Mb/s	8 KHz	5 KHz	300 Hz	34.368 MHz
34 Mb/s	26 KHz	20 KHz	1 KHz	34.368 MHz
34 Mb/s	100 KHz	500 KHz	30 KHz	34.368 MHz
140 Mb/s	2.5 KHz	10 KHz	300 Hz	139.264 MHz
140 Mb/s	10 KHz	50 KHz	3 KHz	139.264 MHz
140 Mb/s	50 KHz	200 KHz	10 KHz	139.264 MHz
STM–0E (52 MHz)	2.5 KHz	10 KHz	300 Hz	51.84 MHz
STM–0E (52 MHz)	5 KHz	20 KHz	1 KHz	51.84 MHz
STM–0E (52 MHz)	10 KHz	50 KHz	3 KHz	51.84 MHz
STM–0E (52 MHz)	26 KHz	100 KHz	3 KHz	51.84 MHz
STM–1E (155 MHz)	5 KHz	20 KHz	1 KHz	155.52 MHz
STM–1E (155 MHz)	10 KHz	50 KHz	3 KHz	155.52 MHz
STM–1E (155 MHz)	26 KHz	100 KHz	3 KHz	155.52 MHz
STM–4 (622 MHz)	10 KHz	50 KHz	3 KHz	622.08 MHz
STM–4 (622 MHz)	68 KHz	200 KHz	10 KHz	622.08 MHz
STM–4 (622 MHz)	600 KHz	2 MHz	100 KHz	622.08 MHz
45Mb/s *(Option 55 only)*	2.3 KHz	10 KHz	300 Hz	44.736 MHz
45Mb/s *(Option 55 only)*	10 KHz	50 KHz	3 KHz	44.736 MHz
45Mb/s *(Option 55 only)*	26 KHz	100 KHz	3 KHz	44.736 MHz
45Mb/s *(Option 55 only)*	60 KHz	200 KHz	10 KHz	44.736 MHz

6. Set up the CTS with the following sequence using the values specified in Table 4-6:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TRANSMIT	TRANSMIT SETTINGS	Transmit Rate *(rotate knob to highlight)*	*as specified in column 1 of Table 4-6*
TRANSMIT	JITTER & WANDER	Jitter/Wander Generation	Off
		Jitter Output	Clock 0.8 V
		Jitter Clock Rate	*as specified in column 1 of Table 4-6*

7. Adjust the spectrum analyzer **Center Frequency** if necessary to center the unjittered signal spectrum.

8. Continue the CTS setup with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TRANSMIT	JITTER & WANDER	Jitter/Wander Generation	On
		Jitter Frequency	*as specified in column 2 of Table 4-6**
		Jitter Amplitude	*as specified in column 3 of Table 4-6 **

*** If the specified value is not one of the available menu choices, choose USER DEFINED, set the value with the knob, and then press DONE.**

NOTE: *During some jitter tests, the front–panel LOS light will turn on. This is a normal condition and not an indication of a failure.*

9. On the spectrum analyzer, observe the measured amplitude at the center frequency (allow the amplitude to stabilize after several sweeps).

10. Increase the generated Jitter Amplitude by the increment listed in column 4 of Table 4-6 using the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TRANSMIT	JITTER & WANDER	Jitter Amplitude	*increase by amount specified in column 4 of Table 4-6*

11. Press **DONE** after each change in jitter amplitude.

12. Repeat steps 9 through 11 until the measured amplitude at the center frequency decreases through its minimum and starts to increase.

13. If the tabulated initial increment (column 4 of Table 4-6) is not 0.01UI, repeat steps 9 and 11 using a 0.01UI increment to find the minimum measured amplitude at the center frequency.

14. Verify that the Jitter Amplitude setting on the CTS, which corresponds to the minimum center–frequency amplitude, is between the limits listed in column 5 of Table 4-6.

Table 4-6. High-Amplitude CTS Generation Setups

COLUMN 1	*COLUMN 2*	*COLUMN 3*	*COLUMN 4*	*COLUMN 5*
Transmit/Clock Rate	**Jitter Frequency**	**Initial Jitter Amplitude**	**Initial Increment**	**Jitter Limits**
2 Mb/s (Unbalanced)	2.5 KHz	1.62 UI	0.02 UI	1.64 to 1.88 UI
2 Mb/s (Unbalanced)	1.8 KHz	8.2 UI	0.1 UI	8.28 to 9.22 UI
2 Mb/s (Unbalanced)	6.4 KHz	2.5 UI	0.05 UI	2.58 to 2.92 UI
34 Mb/s	2.5 KHz	1.62 UI	0.02 UI	1.64 to 1.88 UI
34 Mb/s	8 KHz	8.2 UI	0.1 UI	8.28 to 9.22 UI
34 Mb/s	26 KHz	2.5 UI	0.05 UI	2.58 to 2.92 UI
34 Mb/s	100 KHz	0.68 UI	0.01 UI	0.70 to 0.83 UI
140 Mb/s	2.5 KHz	1.62 UI	0.02 UI	1.63 to 1.89 UI
140 Mb/s	10 KHz	8.2 UI	0.1 UI	8.27 to 9.23 UI
140 Mb/s	50 KHz	2.5 UI	0.05 UI	2.57 to 2.93 UI
STM–0E	2.5 KHz	1.62 UI	0.02 UI	1.64 to 1.88 UI
STM–0E	5 KHz	1.62 UI	0.02 UI	1.64 to 1.88 UI
STM–0E	10 KHz	8.2 UI	0.1 UI	8.28 to 9.22 UI
STM–0E	26 KHz	2.5 UI	0.05 UI	2.58 to 2.92 UI
STM–1E	5 KHz	1.62 UI	0.02 UI	1.63 to 1.89 UI
STM–1E	10 KHz	8.2 UI	0.1 UI	8.28 to 9.22 UI
STM–1E	26 KHz	5.4 UI	0.1 UI	5.42 to 6.08 UI
STM–4	10 KHz *(first test)*	1.55 UI	0.05 UI	1.56 to 1.96 UI
STM–4	10 KHz *(second test)*	8.2 UI	0.1 UI	8.20 to 9.30 UI
STM–4	68 KHz	5.3 UI	0.1 UI	5.35 to 6.15 UI
STM–4	600 KHz	0.6 UI	0.02 UI	0.62 to 0.91 UI
45Mb/s *(Option 55 only)*	2.3 KHz	1.62 UI	0.02 UI	1.63 to 1.89 UI
45Mb/s *(Option 55 only)*	10 KHz	8.2 UI	0.1 UI	8.27 to 9.23 UI
45Mb/s *(Option 55 only)*	26 KHz	2.5 UI	0.05 UI	2.57 to 2.93 UI
45Mb/s *(Option 55 only)*	60 KHz	0.68 UI	0.01 UI	0.69 to 0.84 UI

15. Set up the CTS with the following sequence using values specified in Table 4-7:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TRANSMIT	JITTER & WANDER	Jitter Output	Line
RECEIVE	JITTER & WANDER	Jitter Measurement Range	*as specified in column 3 of Table 4-7*
		Jitter Input Filter	*as specified in column 4 of Table 4-7*
RESULTS	MAIN RESULTS	*none*	Jitter/Wander

16. Press the **START/STOP** button, and verify that the START/STOP light is on.

17. Wait 30 seconds for the test to complete.

18. Verify that the current peak-peak jitter measurement by the CTS is between the limits in column 5 of Table 4-7.

19. Repeat steps 5 through 18 for each row in Tables 4-5, 4-6, 4-7.

Table 4-7: High-Amplitude CTS Measurement Setups

Transmit Rate	Jitter Frequency	Jitter Range	Jitter Filter	Measured Jitter Limits
2 Mb/s (Unbalanced)	2.5 KHz	Normal	Wideband	1.637 to 1.883 UI
2 Mb/s (Unbalanced)	1.8 KHz	Extended	Wideband	8.27 to 9.22 UI
2 Mb/s (Unbalanced)	6.4 KHz	Normal	Wideband	2.577 to 2.922 UI
34 Mb/s	2.5 KHz	Normal	Wideband	1.635 to 1.882 UI
34 Mb/s	8 KHz	Extended	Wideband	8.27 to 9.22 UI
34 Mb/s	26 KHz	Normal	Wideband	2.577 to 2.922 UI
34 Mb/s	100 KHz	Normal	Wideband	0.692 to 0.838 UI
140 Mb/s	2.5 KHz	Normal	Wideband	1.631 to 1.878 UI
140 Mb/s	10 KHz	Extended	Wideband	8.27 to 9.22 UI
140 Mb/s	50 KHz	Normal	Wideband	2.577 to 2.922 UI
STM–0E	2.5 KHz	Normal	Wideband	1.635 to 1.882 UI
STM–0E	5 KHz	Normal	Wideband	1.637 to 1.883 UI
STM–0E	10 KHz	Extended	Wideband	8.27 to 9.22 UI
STM–0E	26 KHz	Normal	Wideband	2.577 to 2.922 UI
STM–1E	5 KHz	Normal	Wideband	1.627 to 1.876 UI
STM–1E	10 KHz	Extended	Wideband	8.27 to 9.21 UI
STM–1E	26 KHz	Normal	Wideband	5.426 to 6.072 UI
STM–4	10 KHz (first test)	Normal	Wideband	1.592 to 1.911 UI
STM–4	10 KHz (second test)	Extended	Wideband	8.19 to 9.22 UI
STM–4	68 KHz	Normal	Wideband	5.392 to 6.107 UI
STM–4	600 KHz	Normal	Highband	0.611 to 0.802 UI
45Mb/s *(Option 55 only)*	2.3 KHz	Normal	Wideband	1.637 to 1.883 UI
45Mb/s *(Option 55 only)*	10 KHz	Extended	Wideband	8.27 to 9.22 UI
45Mb/s *(Option 55 only)*	26 KHz	Normal	Wideband	2.577 to 2.922 UI
45Mb/s *(Option 55 only)*	60 KHz	Normal	Wideband	0.692 to 0.838 UI

This completes the Option 14 Performance Verification Procedure.

Low-Amplitude Jitter Tests

Perform the following setup to prepare for the Low–Amplitude Jitter Tests.

Equipment Required	Spectrum analyzer (item 7) 75 Ohm BNC coaxial cable , three required (item 12) Optical fiber cable (item 8) 75 Ohm to 50 Ohm impedance converter (item 32) N–to–BNC adapter (item 14)
Prerequisites	High Amplitude Jitter Tests
Time Required	Approximately 60 minutes

1. Perform the initial CTS setup with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup
TRANSMIT	TRANSMIT SETTINGS	Tx/Rx Settings	Coupled
TEST SETUPS	TEST CONTROL	Test Duration	USER DEFINED
			Second

2. Rotate the knob to set the Test Duration to 30 seconds, and then press **Done**.

CAUTION: *To prevent damage to the spectrum analyzer, follow the next step carefully before completing the instrument hookup.*

3. Perform the initial setup of the spectrum analyzer with the following steps:
   a. Set the reference level to **0 dBm**.
   b. Set the vertical scale factor to **10 dB/division**.
   c. Set the sweep to **free run**.
   d. Set the sweep to **auto** (or **coupled**).

4. Connect all CTS inputs and outputs in a loop–back configuration. Also, connect the rear–panel jitter clock output (J/CLK) to the spectrum analyzer RF input as shown in Figure 4-41.

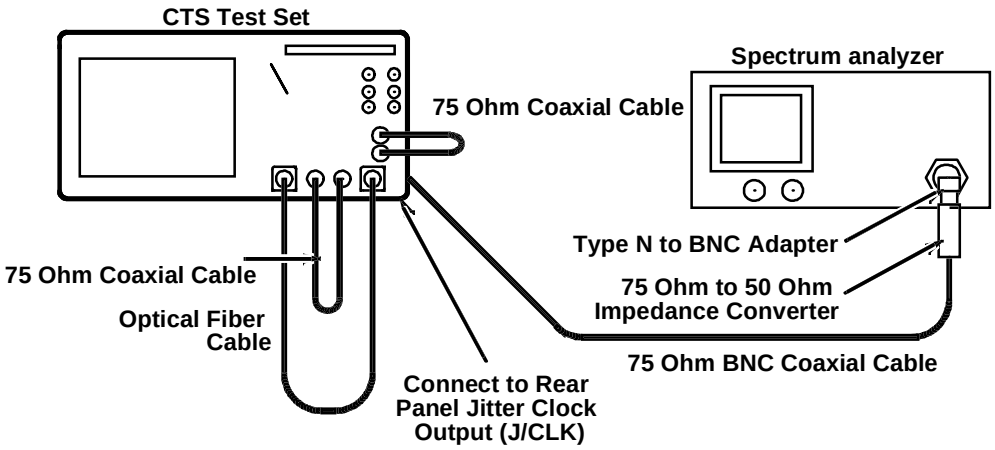


Figure 4-41: Low-Amplitude Jitter Test Hookup

NOTE: *In the next steps, you will repeat a jitter measurement for several jitter frequencies and transmit/receive rates. The basic process is described once. The three tables that follow describe the specific conditions for each test. You will repeat the process for each row in the tables.*

5. For each row in Table 4-8, set up the spectrum analyzer as follows:

   a. Set the span (total over 10 divisions) to the value in column 3 of Table 4-8.

   b. Set both the resolution bandwidth and video bandwidth to the value in column 4 of Table 4-8.

   c. Set the center frequency to the value in column 5 of Table 4-8.

Table 4-8. Low-Amplitude Spectrum Analyzer Setups

Transmit Rate	Jitter Frequency	Ten–Division Span	Resolution Bandwidth and Video Bandwidth	Center Frequency
2 Mb/s (Unbalanced)	50 KHz	200 KHz	10 KHz	2.048 MHz
2 Mb/s (Unbalanced)	100 KHz	500 KHz	30 KHz	2.048 MHz
34 Mb/s	800 KHz	2 MHz	100 KHz	34.368 MHz
140 Mb/s	400 KHz	1 MHz	30 KHz	139.264 MHz
140 Mb/s	3.5 MHz	10 MHz	300 KHz	139.264 MHz
STM–0E	400 KHz	1 MHz	30 KHz	51.84 MHz
STM–1E	650 KHz	2 MHz	100 KHz	155.52 MHz
STM–1E	1.3 MHz	5 MHz	300 KHz	155.52 MHz
STM–4	3 MHz	200 KHz	10 KHz	622.08 MHz
45Mb/s *(Option 55 only)*	400 KHz	2 MHz	100 KHz	44.736 MHz

6. Set up the CTS with the following sequence using the values specified in Table 4-9:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TRANSMIT	TRANSMIT SETTINGS	Transmit Rate	*as specified in column 1 of Table 4-9*
TRANSMIT	JITTER & WANDER	Jitter/Wander Generation	Off
		Jitter Output	Clock 0.8 V
		Jitter Clock Rate	*as specified in column 1 of Table 4-9*
		Jitter Frequency	*as specified in column 2 of Table 4-9 **
		Jitter Amplitude	*as specified in column 3 of Table 4-9 **

*** If the specified value is not one of the available menu choices, choose USER DEFINED, set the value with the knob, and then press DONE.**

7. Adjust the spectrum analyzer **center frequency** if necessary to center the unjittered signal spectrum.

8. Set the spectrum analyzer vertical scale factor to **2 dB/division**.

9. Adjust the spectrum analyzer reference level to set the peak at the center frequency to the top granular line.

10. Continue the CTS setup with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TRANSMIT	JITTER & WANDER	Jitter/Wander Generation	On

11. On the spectrum analyzer display, measure the amplitudes (in dBm) of the center frequency (CF), the first side lobe above the carrier (USL), and the first side lobe below the carrier (LSL).

12. Perform the following calculations on the measured amplitudes:

$$\textit{Side band level (dB)} = \textit{Amplitude}_{USL} + \textit{Amplitude}_{LSL} - (2 \times \textit{Amplitude}_{CF})$$

$$\textit{Jitter (UI)} = (\textit{Side band level} \times 0.01354) + 0.4541$$

13. Verify that the calculated jitter from step 12 is between the limits listed in column 3 of Table 4-9.

Table 4-9. Low-Amplitude CTS Generation Setups

Transmit Rate	Jitter Frequency	Jitter Amplitude	Calculated Jitter Limits
2 Mb/s	50 kHz	0.3 UI	0.255 to 0.345 UI
2 Mb/s	100 kHz	0.5 UI	0.445 to 0.555 UI
34 Mb/s	800 kHz	0.5 UI	0.445 to 0.555 UI
140 Mb/s	400 kHz	0.5 UI	0.445 to 0.555 UI
140 Mb/s	3.5 MHz	0.5 UI	0.445 to 0.555UI
STM–0E	400 kHz	0.5 UI	0.445 to 0.555 UI
STM–1E	650 kHz	0.5 UI	0.445 to 0.555 UI
STM–1E	1.3 MHz	0.4 UI	0.350 to 0.450 UI
STM–4	3 MHz	0.3 UI	0.225 to 0.375 UI
45Mb/s *(Option 55 only)*	400 KHz	0.50 UI	0.435 to 0.565 UI

14. Set up the CTS with the following sequence using values specified in Table 4-10:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TRANSMIT	JITTER & WANDER	Jitter Output	Line
RECEIVE	JITTER & WANDER	Jitter Measurement Range	*as specified in column 3 of Table 4-10*
		Jitter Input Filter	*as specified in column 4 of Table 4-10*
RESULTS	MAIN RESULTS	*none*	Jitter/Wander

15. Press the **START/STOP** button, and verify that the START/STOP light is on.

16. Wait 30 seconds for the test to complete.

17. Calculate the minimum and maximum jitter limits. To do this, start with the calculated jitter result from step 12, and then add or subtract the amounts shown in columns 5 and 6 of Table 4-10.

18. Verify that the current peak–to–peak jitter measurement by the CTS is within the jitter limits calculated in step 17.

19. Repeat steps 5 through 18 for each row in Tables 4-8, 4-9, 4-10.

Table 4-10: Low-Amplitude CTS Measurement Setups

Transmit Rate	Jitter Frequency	Jitter Range	Jitter Filter	Minimum Jitter Limit *	Maximum Jitter Limit *
2 Mb/s (Unbalanced)	50 kHz	Normal	Wideband	J - 0.061 UI	J + 0.049 UI
2 Mb/s (Unbalanced)	100 kHz	Normal	Highband - National	J - 0.151 UI	J + 0.029 UI
34 Mb/s	800 kHz	Normal	Highband	J - 0.207 UI	J + 0.077 UI
140 Mb/s	400 kHz	Normal	Wideband	J - 0.062 UI	J + 0.068 UI
140 Mb/s	3.5 MHz	Normal	Highband	J - 0.207 UI	J + 0.077 UI
STM–0E	400 kHz	Normal	Highband	J - 0.207 UI	J + 0.077 UI
STM–1E	650 kHz	Normal	Highband	J - 0.067 UI	J + 0.063 UI
STM–1E	1.3 MHz	Normal	Wideband	J - 0.207 UI	J + 0.077 UI
STM-4	3 MHz	Normal	Wideband	J - 0.101 UI	J + 0.079 UI
45Mb/s *(Option 55 only)*	400 KHz	Normal	Highband	J – 0.207 UI	J + 0.077 UI

*** The variable "J" refers to the calculated jitter result from step 12.**

Adjustment Procedures

This section contains information needed to adjust the CTS. There are only three types of adjustments you can perform on the CTS. Table 5-1 lists the adjustments and when they are required.

Table 5-1: When to Adjust the CTS

Adjustment	Routine Adjustment	Adjustment After Repair
Setting the CTS serial number	Not required	After replacing the CPU board
Adjusting the internal clock frequency	Only if the clock frequency is out of tolerance	After replacing the Clock board or Low–Voltage Power Supply
Adjusting the display monitor	Not required	After replacing the monitor or the Low–Voltage Power Supply
Calibrating jitter generation and measurement (Option 14 only)	Before taking critical measurements	After replacing JAWA/JAWG assembly, Tributary assembly, or Plug–in Interface Module.

Equipment Required

The tools and test equipment needed to adjust the CTS are listed in Table 5-2. Setting the serial number or adjusting the internal clock frequency requires communication with the CTS through its GPIB or RS–232 port. There are several ways to set up bus communication:

- Connect a terminal or a PC with a terminal–emulator program to the CTS RS–232 port.
- Connect a GPIB controller with talker/listener software to the CTS GPIB port.
- If you have a Tektronix VX4610 and a PC controller, you can use the UI4610 Software, a standard accessory of the VX4610, to communicate with your CTS. The UI4610 Software contains a GPIB talker/listener tool.

Table 5-2: Required Tools and Equipment for Adjustment

Item Number and Description		Minimum Requirements	Example	Purpose
1	Universal Counter/Timer	60 MHz frequency measurement capability; 0.25 ppm time base accuracy; 9 digits; averaging to 10^8	Tektronix DC 5010 Digital Counter/Timer with TM 5000 mainframe	Adjusting the internal clock frequency
2	50 Ω SMB–to–BNC Coaxial Cable	50 Ω impedance; SMB female connector on one end, BNC male connector on the other	Tektronix P6041	Adjusting the internal clock frequency
3	External Graticule Test Fixture	Tektronix part number 067–0206–01	Tektronix part number 067–0206–01	Adjusting display monitor size and position
4	Photometer	0.1 to 200 fL	Tektronix J17 LumaColor Photometer with J1803 Luminance Head	Adjusting display monitor brightness and contrast
5	Terminal, Terminal Emulator, or Controller	RS–232 or GPIB talker/listener capability	PC controller with Tektronix UI4610 software (standard accessory to VX4610)	Setting the serial number Adjusting the internal clock frequency
6	Adjustment Tool	0.075 inch slotted screwdriver	Tektronix part number 003–1433–01 (standard probe adjustment tool)	Adjusting the internal clock frequency Adjusting the display monitor
7	Flat–Bladed Screwdriver	General purpose, 0.25 inch, slotted screwdriver	Xcelite R–144	Adjusting the internal clock frequency

Procedures

The following adjustment procedures are independent of one another and may be performed in any order. Allow the CTS a 20–minute warm–up period before performing any adjustments.

Setting the Serial Number

Use this procedure to set the CTS serial number after you have replaced the CPU board.

Equipment Required	Terminal, Terminal Emulator, or Controller (item 5)
Time Required	Approximately five minutes

1. Connect the terminal, terminal emulator, or controller to the RS–232 or GPIB port on the rear panel of the CTS. Set the communication port parameters as needed to establish communication. The CTS communication port settings are accessible with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
UTILITY	REMOTE CONTROL	*as needed*	*as needed*

2. Using the terminal or controller, send the following command (substitute the actual serial number for the parameter <s/n>):

   ```
   SYSTem:SERIal " <s/n>" ;
   ```

   For example, to set the serial number to B010100, send the command `SYSTem:SERIal " B010100" ;`.

3. Display the serial number with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
UTILITY	INSTR CONFIG	*none*	*none*

4. Verify that the displayed serial number is correct. If so, you have completed this procedure. If it is not correct, reverify the communication between the terminal or controller and the CTS and repeat the procedure.

Adjusting the Internal Clock Frequency

You should adjust the internal clock frequency only if you have replaced the Clock board, replaced the Low–Voltage Power Supply, or if the internal clock frequency is out of tolerance. You should perform this adjustment if the CTS fails the physical layer test *Checking Internal Clock Accuracy*.

Equipment Required	Universal Counter/Timer (item 1) SMB–to–BNC Coaxial Cable (item 2) Terminal, Terminal Emulator, or Controller (item 5) Adjustment Tool (item 6) Flat–Bladed Screwdriver (item 7)
Time Required	Approximately one hour

1. Connect the terminal, terminal emulator, or controller to the RS–232 or GPIB port on the rear panel of the CTS. Set the communication port parameters as needed to establish communication. The CTS communication port settings are accessible with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
UTILITY	REMOTE CONTROL	*as needed*	*as needed*

2. Connect the SMB–to–BNC coaxial cable from the CAL output on the CTS rear panel to the Universal Counter/Timer as shown in Figure 5-1.

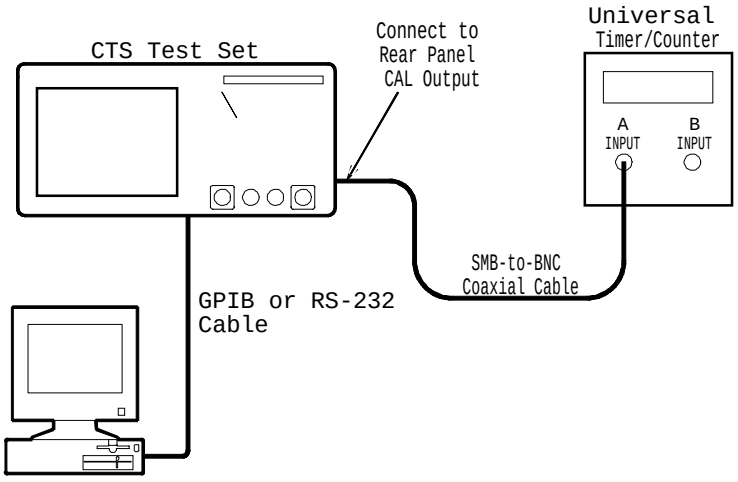


Figure 5-1: Internal Clock Frequency Adjustment Connections

3. Using the terminal or controller, send the following command:

```
DIAGnostic:CALIbrate:CLOCk 0.0;
```

4. To measure the internal clock frequency, set up the CTS with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
TEST SETUPS	RECALL INSTRUMENT SETUPS	DEFAULT FACTORY SETTINGS	Recall Setup

5. Set the Universal Counter/Timer as follows:
   a. Set input impedance to **50 Ohm.**
   b. Set input coupling to **AC**.
   c. Set number of averages to $\mathbf{10^8}$.
   d. Set measurement mode to **Frequency**.
6. Verify that the Universal Counter/Timer reads between 51,839,960 Hz and 51,840,238 Hz (inclusive). If it does, the internal clock frequency is within tolerance and you have completed this procedure. Proceed to step 7 only if the internal clock frequency is out of tolerance.
7. Turn off power to the CTS, disconnect it from the test setup, and unplug the power cord from the AC source.
8. To adjust the CTS internal clock frequency, you must remove the line cord, rear cover, and cabinet.

WARNING. High voltages are accessible on the power supply and the monitor assembly. Do not touch these circuit boards when the power is on.

9. After the cabinet has been removed, reconnect the CTS to the setup shown in Figure 5-1, reconnect the line cord, apply power, and allow the CTS to warm up again for at least 20 minutes.
10. When the warm–up is complete, locate the crystal oscillator on the right side of the CTS (see Figure 5-2).

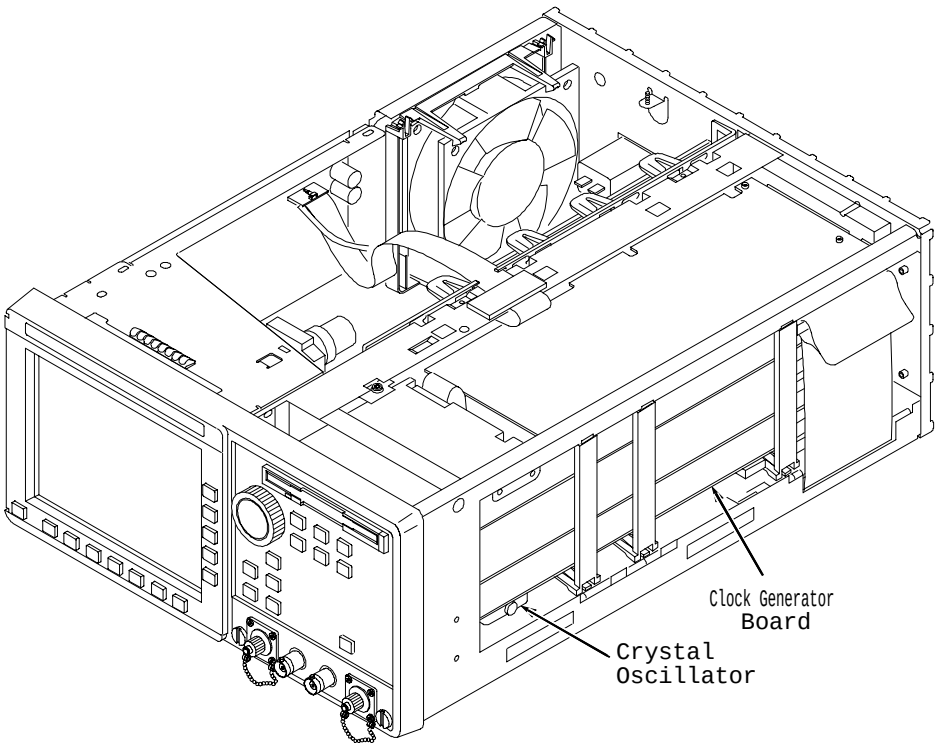


Figure 5-2: Location of Crystal Oscillator

11. Using the flat–bladed screwdriver, carefully remove the slotted screw on the side of the crystal oscillator to access the adjustment screw.

12. Insert the adjustment tool into the crystal and adjust the internal clock frequency to 51,840,000 Hz ± 10 Hz.

13. Replace the slotted screw that covers the crystal oscillator adjustment screw.

14. Using the terminal or controller, send the following command to set the clock calibration date, where `yy,mm,dd` is the current year, month, and day:

```
DIAGnostic:CALIbrate:CDAT yy,mm,dd;
```

15. The internal clock adjustment is complete. Turn off power and reassemble the CTS.

Adjusting the Display Monitor

You should perform these adjustments only if you have replaced the monitor, replaced the Low–Voltage Power Supply, or if the display quality is unsatisfactory.

Equipment Required	External Graticule Test Fixture (item 3) Photometer (item 4) Adjustment Tool (item 6) Flat–Bladed Screwdriver (item 7)
Time Required	Approximately one hour

1. To adjust the display monitor, you must remove the line cord, rear cover, and cabinet.

WARNING. High voltages are accessible on the power supply and the monitor assembly. Do not touch these circuit boards when the power is on. Do not touch the CRT anode button even if the power is off. Wear safety glasses when working with the CRT.

2. After the cabinet has been removed, reconnect the CTS to the setup shown in Figure 5-1, reconnect the line cord, apply power, and allow the CTS to warm up for at least 20 minutes.
3. To prepare the J17 LumaColor Photometer to make measurements, perform the following steps:
   a. With the photometer power turned off, connect the J1803 Luminance Head to the photometer.
   b. Turn the photometer power on. The photometer performs a brief self test.
   c. Press the **ALT DISP** button once and the **UNITS** button once.
   d. Verify that the photometer displays the letters WHT in the upper–left corner, the letters fL in the upper–right corner, and a four–digit number in the center. If the display does not contain this information, turn off the power and repeat steps b through d.
4. Locate the monitor adjustments along the top–left side of the CTS (see Figure 5-3).

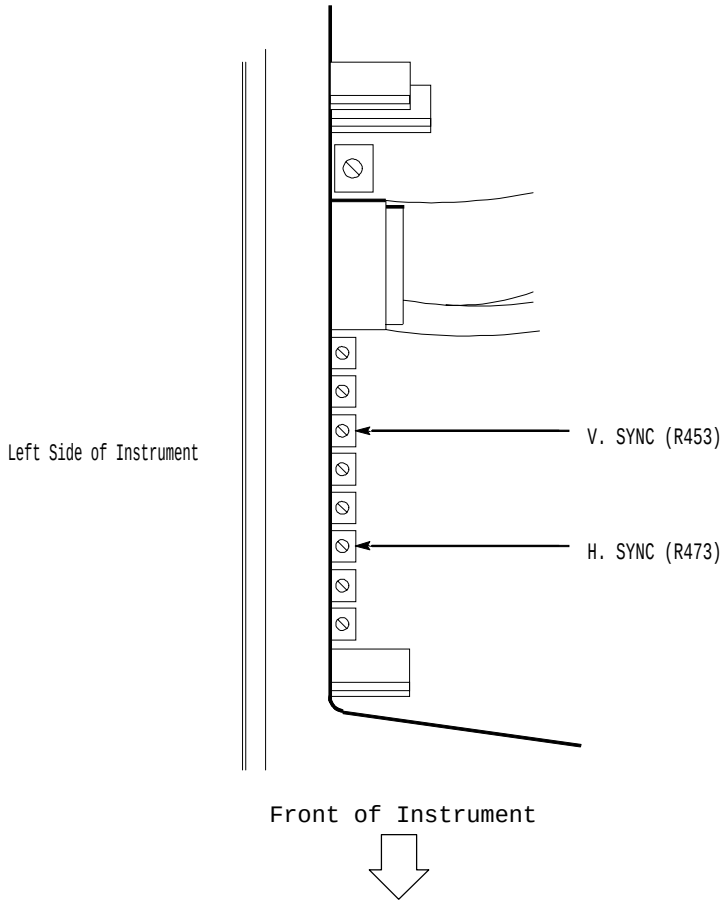


Figure 5-3: Monitor Adjustment Locations

5. To adjust the vertical and horizontal sync, perform the following steps:

a. If the display rolls vertically, adjust **V. SYNC (R453)** to the center of the stable display range.

b. If diagonal lines are present on the display, adjust **H. SYNC (R473)** to the center of the stable display range.

6. To adjust the display brightness, perform the following steps:

a. Set the CTS to display a gray field pattern (see Figure 5-4) with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
UTILITY	SELF TEST	Self Test Group	DISPLAY
		Self Test Routine	Gray Field
		Self Test Control	RUN

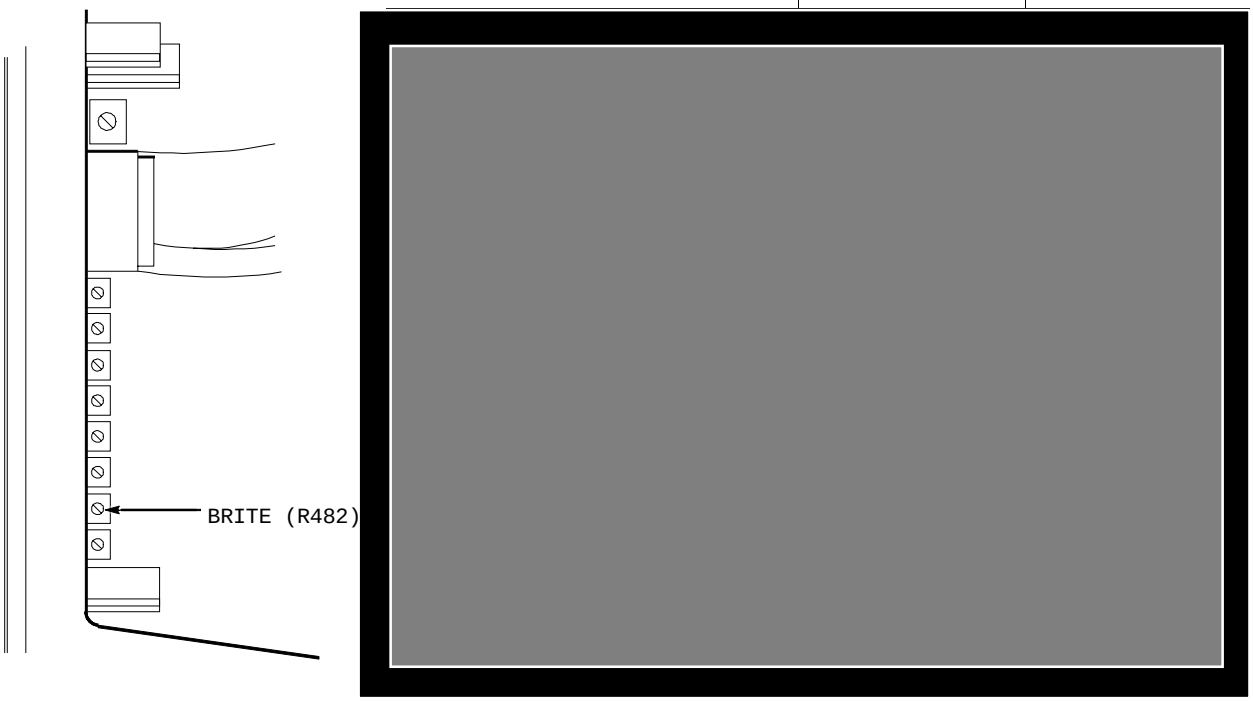


Figure 5-4: Brightness Adjustment and Gray Field Pattern

b. Hold the J1803 Luminance Probe against the faceplate of the monitor at the center of the screen.

c. Verify that the display brightness is within the tolerance from 1.4 fL to 2.1 fL (inclusive).

d. If the display brightness is out of tolerance, adjust **BRITE (R482)** for a reading of approximately 1.75 fL.

7. To adjust video gain perform the following steps:

a. Set the CTS to display a white box pattern (see Figure 5-5) with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
UTILITY	SELF TEST	Self Test Group	DISPLAY
		Self Test Routine	White Box
		Self Test Control	RUN

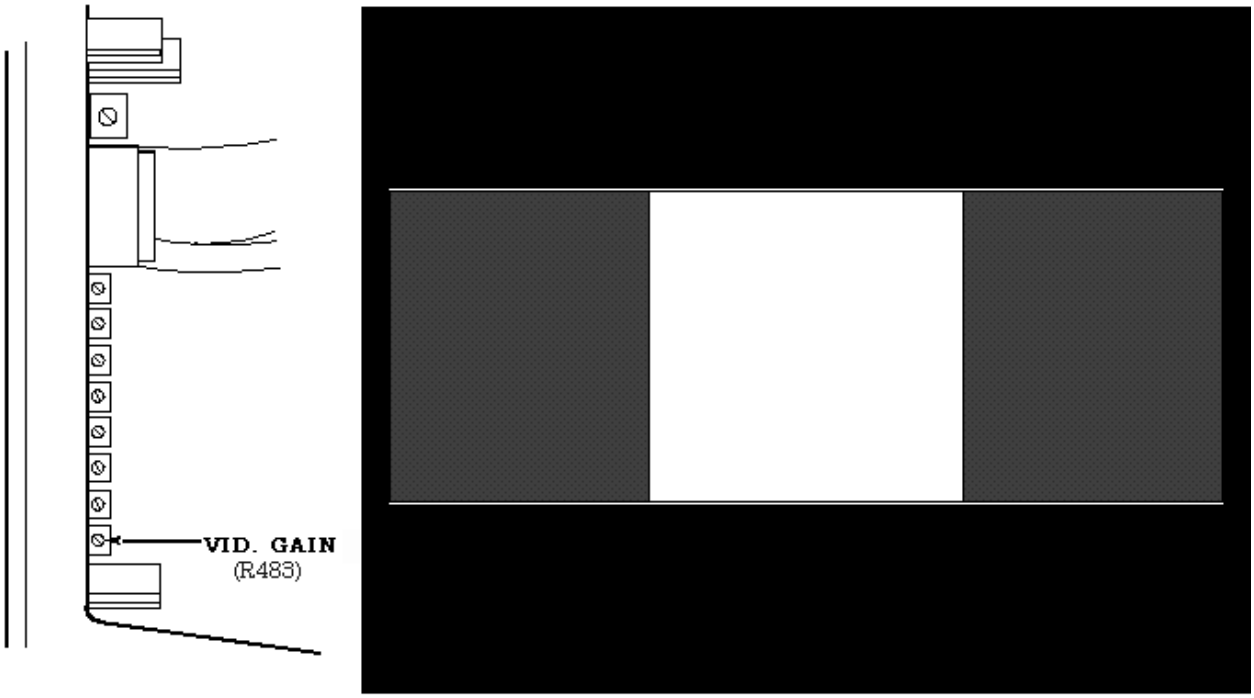


Figure 5-5: Video Gain Adjustment and White Box Pattern

b. Hold the J1803 Luminance Probe against the faceplate of the monitor at the center of the screen.

c. Verify that the display brightness is within the tolerance from 35 fL to 53 fL (inclusive).

d. If the display brightness is out of tolerance, adjust **VID. GAIN (R483)** for a reading of approximately 44 fL.

e. If you adjusted the video gain, repeat steps 6 and 7 until both the brightness and video gain measurements are within tolerance.

8. To adjust the display focus, perform the following steps:

a. Set the CTS to display a composite test pattern (see Figure 5-6) with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
UTILITY	SELF TEST	Self Test Group	DISPLAY
		Self Test Routine	Composite
		Self Test Control	RUN

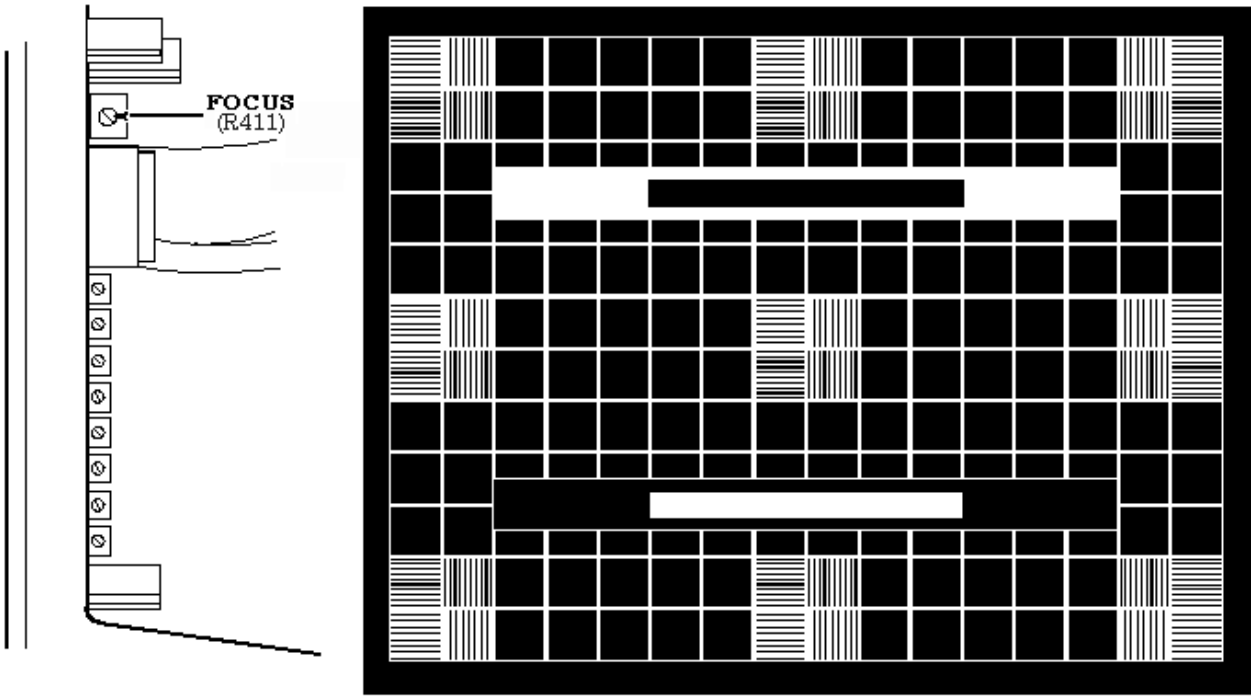


Figure 5-6: Focus Adjustment and Composite Test Pattern

b. Adjust **FOCUS (R411)** for best overall focus at all four corners and at the center of the screen.

c. Press any CTS front–panel button to continue.

9. To adjust the display position and size, perform the following steps:

a. Set the CTS to display a test grid pattern (see Figure 5-7) with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
UTILITY	SELF TEST	Self Test Group	DISPLAY
		Self Test Routine	Test Grid
		Self Test Control	RUN

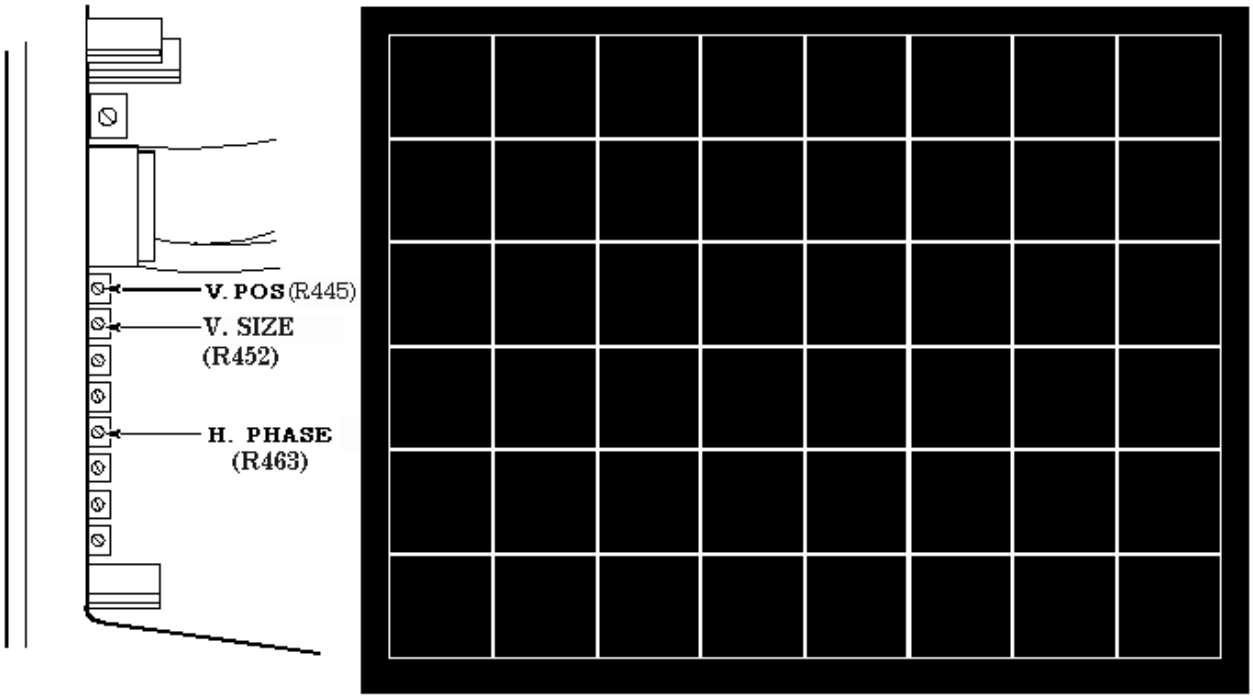


Figure 5-7: Position and Size Adjustments and Test Grid Pattern

b. To make the following adjustments, use the External Graticule Test Fixture as a visual reference (see Figure 5-8). You can position the test fixture in the CTS bezel opening as necessary to align it to the displayed test pattern. Start by positioning the External Graticule Test Fixture so that it is centered (approximately) in the bezel opening.

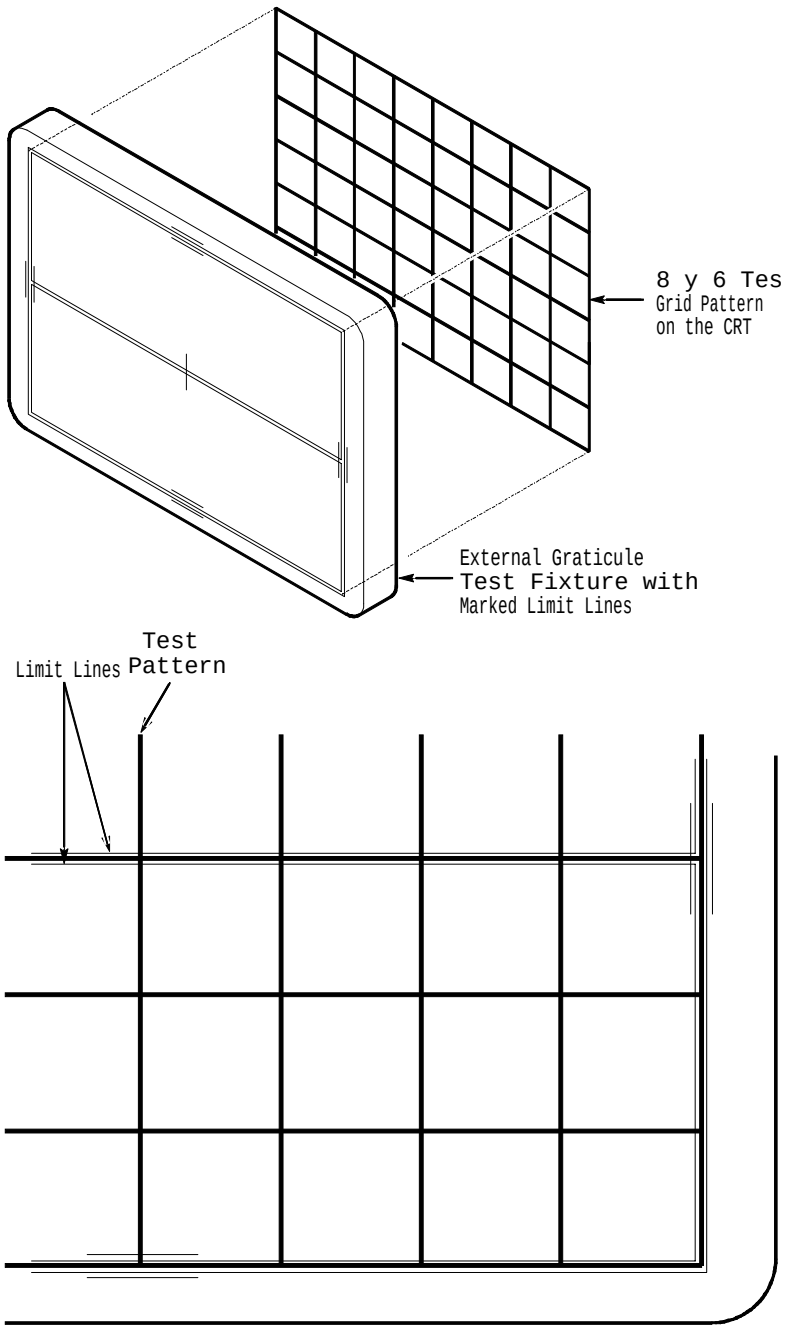


Figure 5-8: External Graticule Limit Lines

c. Adjust **V. POS (R445)** so that the horizontal centerline is within the limit lines of the External Graticule Test Fixture. (See Figure 5-8.) You may need to rotate the External Graticule Test Fixture slightly to see the horizontal centerline within its limits across the entire display.

d. Adjust **V. SIZE (R452)** so that the top and bottom lines are within their limits. You can reposition the External Graticule Test Fixture as necessary to make this adjustment.

e. Reposition the External Graticule Test Fixture so that it is centered (approximately) in the CTS bezel opening.

f. Adjust **H. PHASE (R463)** so that the left and right lines are within their limits. You may need to rotate the External Graticule Test Fixture slightly to see the left and right lines within their limits across the entire display. If you cannot set both lines within their limits, adjust for best compromise.

10. The display monitor adjustment is complete. Turn off power and reassemble the CTS.

Calibrating Jitter Generation and Measurement

For Option 14 equipped test sets only, periodic calibration of the jitter generation and measurement systems is recommended to maintain best accuracy. You can execute built–in calibration routines before making critical measurements.

Equipment Required	None
Time Required	Approximately 90 minutes

To calibrate the jitter generation system:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
UTILITY	CALIBRATION	Calibration System	Jitter Generation
		Calibration Routine	All
		Calibration Control	Run

To calibrate the jitter measurement system:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
UTILITY	CALIBRATION	Calibration System	Jitter Measurement
		Calibration Routine	All
		Calibration Control	Run

A status message indicates that the calibration is running, has completed and has passed, or has failed. Select **Abort** to stop a calibration in progress.

Maintenance

This section contains the information needed to do periodic and corrective maintenance on the CTS 850 SDH/PDH Test Set. The following sections are included:

Preparation -- General information on preventing damage to internal modules when doing maintenance.

Inspection and Cleaning -- Information and procedures for inspecting the CTS850 and cleaning its external and internal modules.

Removal and Replacement -- Instructions for the removal of defective modules and replacement with new or repaired modules. Also included are instructions for disassembly of the CTS850 for cleaning.

Troubleshooting -- Information for isolating and troubleshooting failed modules. Included are troubleshooting trees and instructions for operating the CTS850 internal diagnostic routines.

After–Repair Adjustments -- List of which adjustment procedures you must perform after a module is replaced.

Repackaging Instructions -- Instructions on how to package the CTS850 for shipment.

Preparation

Procedures in this manual are for qualified service personnel only. Before performing any service procedures, read the safety summaries at the front of this manual. Read *Operating Information* before servicing the CTS850.

Related Maintenance Procedures

Refer to these other sections for additional information and procedures related to doing maintenance:

Operating Information contains instructions that you may find useful during service procedures.

Theory of Operation contains a circuit description at the module level.

Performance Verification can help isolate faulty modules by testing CTS850 performance.

Adjustment Procedures addresses after–repair adjustments to the CTS850. It contains a procedure for adjusting the CTS850 internal circuits.

Diagrams contains a block diagram using individual modules as blocks and an interconnect diagram showing connections between the modules.

Mechanical Parts List contains a list of field replaceable modules by part number.

Preventing ESD Damage

When performing any service that requires internal access to the CTS850, follow these precautions to prevent electrostatic discharge (ESD) damage to internal modules and their components:

CAUTION: *Static discharge can damage any semiconductor component in this CTS850 SDH/PDH Test Set.*

1. Minimize handling of static–sensitive modules.
2. Transport and store static–sensitive modules in their static–protected containers. Label any package that contains static–sensitive modules.
3. Discharge the static voltage from your body by wearing a grounded antistatic wrist strap while handling these modules. Perform service of static–sensitive modules only at a static–free work station.
4. Do not remove the CTS850 cabinet unless you have met precaution #3, above. Consider all internal modules static–sensitive.
5. Nothing capable of generating or holding a static charge should be allowed on the work station surface.
6. Handle circuit boards by their edges when possible.
7. Do not slide the modules over any surface.
8. Avoid handling modules in areas that have a floor or work–surface covering capable of generating a static charge.
9. Do not use high–velocity compressed air when cleaning dust from modules.

Inspection and Cleaning

Inspection and Cleaning describes how to inspect for dirt and damage and how to clean the exterior and interior of the CTS850. You should perform inspection and cleaning as preventive maintenance. Preventive maintenance, when done regularly, may prevent CTS850 malfunction and enhance its reliability.

How often to do maintenance depends on the severity of the environment in which you use the CTS850. A proper time to perform preventive maintenance is just before CTS850 adjustment.

General Care

The cabinet helps keep dust out of the CTS850 and is a major component of its cooling system. It should normally be in place when operating the CTS850. The optional CTS850 front cover protects the front panel and display from dust and damage. Install the front cover when storing or transporting the CTS850.

Inspection and Cleaning Procedures

Inspect and clean the CTS850 as often as operating conditions require. The collection of dirt on components inside can cause them to overheat and break down. (Dirt acts as an insulating blanket, preventing efficient heat dissipation.) Dirt also provides an electrical conduction path that could cause a CTS850 failure, especially under high–humidity conditions.

CAUTION. *Avoid the use of chemical cleaning agents that might damage the plastics used in this CTS850. Use only deionized water when cleaning the menu buttons or front–panel buttons. Use a 75% isopropyl alcohol solution as a cleaner and rinse with deionized water. Before using any other type of cleaner, consult your Tektronix Service Center or representative.*

Avoid the use of high pressure compressed air when cleaning dust from the interior of the CTS850. (High pressure air can cause electrostatic discharge.) Instead, use low pressure compressed air (about 9 psi).

Inspection - Exterior

Inspect the outside of the CTS850 for damage, wear, and missing parts using Table 6-1 as a guide. You should thoroughly check a CTS850 that appears to have been dropped or otherwise abused to verify correct operation and performance. Immediately repair defects that could cause personal injury or lead to further damage to the CTS850.

Table 6-1: External Inspection Check List

Item	Inspect For	Repair Action
Cabinet, front panel, and cover	Cracks, scratches, deformations, damaged hardware or gaskets.	Replace defective module.
Front–panel knobs	Missing, damaged, or loose knobs.	Repair or replace missing or defective knobs.
Connectors	Broken shells, cracked insulation, and deformed contacts. Dirt in connectors.	Replace defective modules. Clear or wash out dirt.
Carrying handle and cabinet feet	Correct operation.	Replace defective module.
Accessories	Missing items or parts of items, bent pins, broken or frayed cables, and damaged connectors.	Replace damaged or missing items, frayed cables, and defective modules.

Cleaning Procedure - Exterior

Clean the exterior of the CTS850 as follows:

WARNING: *To avoid injury or death, unplug the power cord from line voltage before cleaning the CTS850. To avoid getting moisture inside the CTS850 during external cleaning, use only enough liquid to dampen the cloth or applicator.*

1. Remove loose dust on the outside of the CTS850 with a lint–free cloth.
2. Remove remaining dirt with a lint–free cloth dampened in a general purpose detergent–and–water solution. Do not use abrasive cleaners.
3. Clean the monitor screen with a lint–free cloth dampened with either isopropyl alcohol or, preferably, a gentle, general purpose detergent–and–water solution.

Cleaning Procedure - Optical Ports

If the CTS850 performance appears degraded, the optical fiber and optical port may be dirty. Clean the fiber connector with a clean cloth.

To clean an optical port:

1. Verify that the CTS has been turned off with the principal power switch on the rear panel.
2. Remove the four screws that attach the bulkhead connector to the front panel (see Figure 6-1).
3. Gently pull the bulkhead out of the unit and unscrew the fiber connector. Be careful not to pull beyond the fiber slack.
4. Using a soft, lint–free cloth with a high–quality glass cleaner, clean the tip of the fiber cable.
5. If available, use low–pressure compressed air or canned air to blow any dirt out of the bulkhead connector. If compressed air is not available, then the bulkhead will have to be taken apart and cleaned. Refer to the removal and replacement procedure *Optical Port Connector*, for information about bulkhead disassembly.
6. After cleaning the bulkhead, reconnect the fiber and install the bulkhead. Be sure to reinstall the dustcap chain.

NOTE: *To keep cleaning to a minimum, install the dustcap when the optical port does not have a fiber attached.*

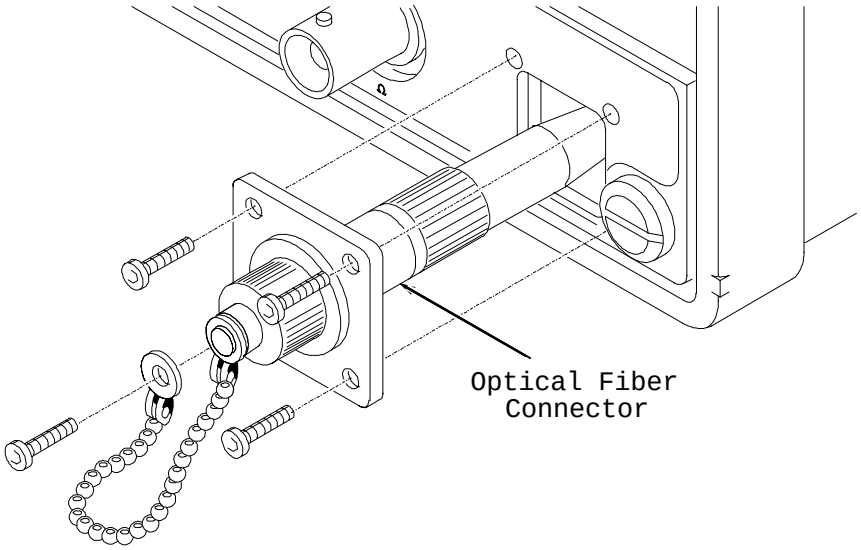


Figure 6-1: Removing the Optical Bulkhead Connector

Inspection - Interior

To access the inside of the CTS850 for inspection and cleaning, refer to *Removal and Replacement*, following this section.

Inspect the internal portions of the CTS850 for damage and wear, using Table 6-2 as a guide. You should repair defects immediately.

If you replace any electrical module, perform the necessary adjustment procedures found in the *Adjustment Procedures* section.

CAUTION. *To prevent damage from electrical arcing, ensure that circuit boards and components are dry before applying power to the CTS850.*

Table 6-2: Internal Inspection Check List

Item	Inspect For	Repair Action
Circuit boards	Loose, broken, or corroded solder connections. Burned circuit boards. Burned, broken, or cracked circuit–run plating.	Replace the failed module.
Solder connections	Cold solder or rosin joints.	Resolder joint and clean with isopropyl alcohol.
Wiring and cables	Loose plugs or connectors. Burned, broken, or frayed wiring.	Firmly seat connectors. Repair or replace modules with defective wires or cables.
Chassis	Dents and deformations	Straighten, repair, or replace chassis.

Cleaning Procedure - Interior

The interior cleaning procedure is as follows:

1. Blow off dust with dry, low–pressure, deionized air (approximately 9 psi).
2. Remove any remaining dust with a lint–free cloth dampened in isopropyl alcohol (75% solution) and rinse with warm deionized water. (A cotton–tipped applicator is useful for cleaning in narrow spaces and on circuit boards.)

NOTE: *If, after doing steps 1 and 2, a module is clean upon inspection, skip steps 3 through 7.*

If steps 1 and 2 do not remove all the dust or dirt, the CTS850 may be spray washed using a solution of 75% isopropyl alcohol by doing steps 3 - 7.

3. Gain access to the parts to be cleaned by removing easily accessible shields and panels (see *Removal and Replacement* section*)*.
4. Spray wash dirty parts with the isopropyl alcohol and wait 60 seconds for the majority of the alcohol to evaporate.
5. Use hot (120° F to 140° F, 49° C to 60° C) deionized water to thoroughly rinse the parts.
6. Dry all parts with low–pressure, deionized air.
7. Dry all components and assemblies in an oven or drying compartment using low–temperature (125° F to 150° F, 52° C to 66° C) circulating air.

Lubrication

There is no periodic lubrication required.

Removal and Replacement

This section contains the following information:

- Preparatory information
- A list of equipment required to remove and disassemble all modules
- Module locator diagrams for finding the modules in the CTS850
- Procedures for removal and replacement of the modules

Preparation

WARNING. *Before doing this or any other procedure in this manual, read the safety summaries found at the beginning of this manual. Also, to prevent possible injury to personnel or damage to the CTS850 SDH/PDH Test Set components, read* ***Supplying Operating Power*** *and* ***Preventing ESD****.*

Before doing any procedure in this section, disconnect the power cord from the line voltage source. Failure to do so could cause serious injury or death.

Read these general instructions before removing a module:

1. Read the *Summary of Procedures* to understand how the procedures are grouped. Then read *Equipment Required* for a list of the tools needed to remove and install modules in the CTS850.
2. Study Figure 6-2, which defines the sides of the CTS850 referred to by the procedures.
3. If you are removing a module for service, begin by doing the *Access Procedure*. By following the instructions in that procedure, you remove the module to be serviced while removing the minimum number of additional modules.
4. If you are disassembling the CTS850 for cleaning, go to the *Disassembly for Cleaning* procedure at the end of this section.

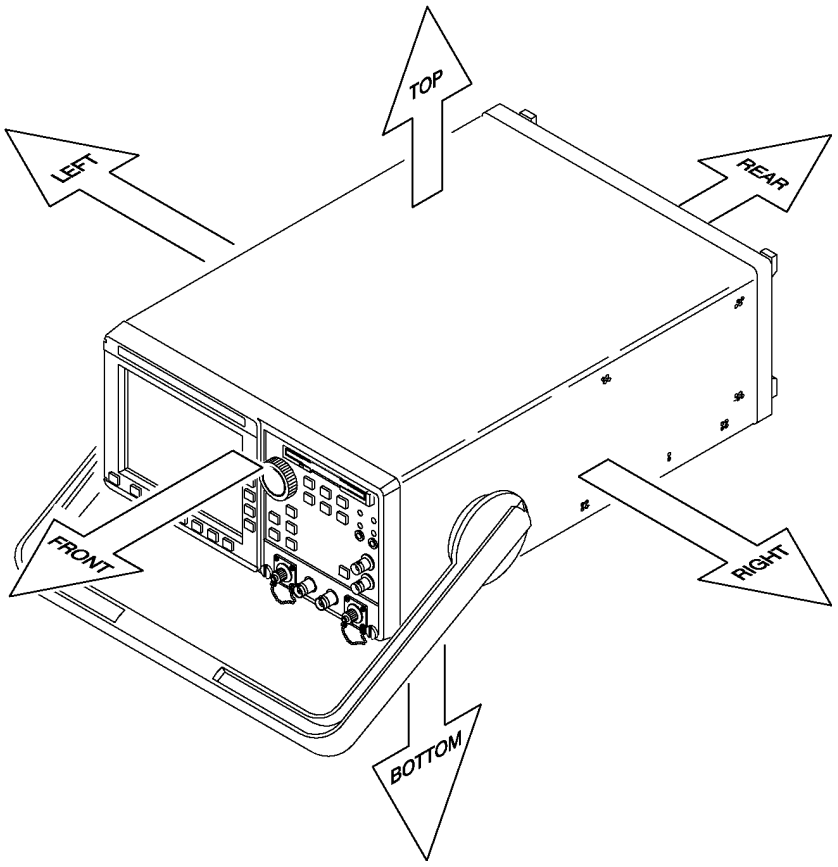


Figure 6-2: CTS 850 Test Set Orientation

Summary of Procedures

The procedures are described in the order in which they appear in this section. These procedures are also listed in the *Table of Contents*.

The *Access Procedure* first directs you to the procedures that remove any modules that must be removed to access the module to be serviced. It then directs you to the procedure to remove that module.

Procedures for Module Removal and Installation are the procedures for removing modules. These procedures assume you have done the access procedure.

Disassembly for Cleaning is a procedure, based on the module removal procedures just described, that removes all modules for cleaning. Instructions for cleaning are found in *Inspection and Cleaning.* The *Disassembly for Cleaning* procedure does not use the access procedure.

Equipment Required

The following tools are required to completely disassemble the CTS850 into its modules. The tools required to remove an individual module are listed in the first step of its procedure. All the tools are standard tools readily available from tool suppliers.

Table 6-3: Tools Required for Module Removal

Item No.	Name	Description
1	Screwdriver handle	Accepts Torx–driver bits.
2	T–15 Torx tip	Torx–driver bit for T–15 size screw heads.
3	T–20 Torx tip	Torx–driver bit for T–20 size screw heads. Used only for removal of the cabinet handle.
4	Flat–bladed screwdriver	Screwdriver for removing standard–head screws.
5	Needle–nose pliers	Standard tool. Used for removing EMI gaskets.
6	Duck–bill pliers	4 inch. Used for removing the Low–Voltage Power Supply.
7	Pozidriv screwdriver	Used for removing disk drive.
8	Nut driver, 5/16 inch	Used for removing earth ground cables.
9	Nut driver, 3/16 inch	Used for removing GPIB connector shell and EMI gasket.
10	Nut driver, 1/4 inch	Used for removing A09 Main Protocol assembly.
11	Nut driver, 9/32 inch	Used for removing EMI gasket.
12	Hex key screwdriver, 1/16 inch	Used for knob removal.
13	Flat–bladed spudger	A probe–like tool, made of wood or fiber, with a tip like a flat bladed screwdriver. Used to press EMI gaskets into place.
14	Slip–jaw pliers	Used for removing the front feet from the cabinet.
15	Soldering iron	15 W. Used for removal of some cables.
16	CTS 850 SDH/PDH Test Set Front Cover	This cover protects the front of the CTS850 SDH/PDH Test Set when positioned face down in the removal procedures.

Table 6-4: Access Instructions for Modules in Figure 6-3

Procedure Including Module to be Removed	Page No.	Access Instructions
Optical Port Connector	6-20	1 Do only the procedure listed at left.
Front–Panel Knob	6-22	1 Do only the procedure listed at left.
Line Fuse	6-24	1 Do only the procedure listed at left.
Front Cover, Rear Cover, Cabinet, Rear EMI Gasket, and Cabinet Handle and Feet	6-26	1 Do the procedure listed at left, removing only the module(s) you want to service. When doing the procedure listed at left, do not remove the rear EMI gasket unless it is being replaced.
Trim Ring, Menu Elastomer, Menu Buttons, and Front EMI Gaskets	6-28	1 Do *Front Cover, Rear Cover, Cabinet, Rear EMI Gasket, and Cabinet Handle and Feet*, removing only the front cover, rear cover, and cabinet. 2 Do the procedure listed at left, removing all modules including the module(s) you want to service. When doing the procedure listed at left, do not remove the front EMI gaskets unless they are being replaced.
Plug–In Interface Module	6-31	1 Do the procedure listed at left, removing the module you want to service.
Disk Drive	6-32	1 Do the *Front Cover, Rear Cover, Cabinet, Rear EMI Gasket, and Cabinet Handle and Feet*, removing only the front cover, rear cover, and cabinet. 2 Do the procedure listed at left to remove the module.
A06 Front Panel Assembly and Menu Flex Circuit	6-33	1 Do *Disk Drive*. 2 Do *Trim Ring, Menu Elastomer, Menu Buttons, and Front EMI Gaskets*. 3 Do *Plug–In Interface Module*. 4 Do the procedure listed at left, removing all modules including the module(s) you want to service. When doing the procedure listed at left, do not remove the menu flex circuit unless it is being replaced with a new module.

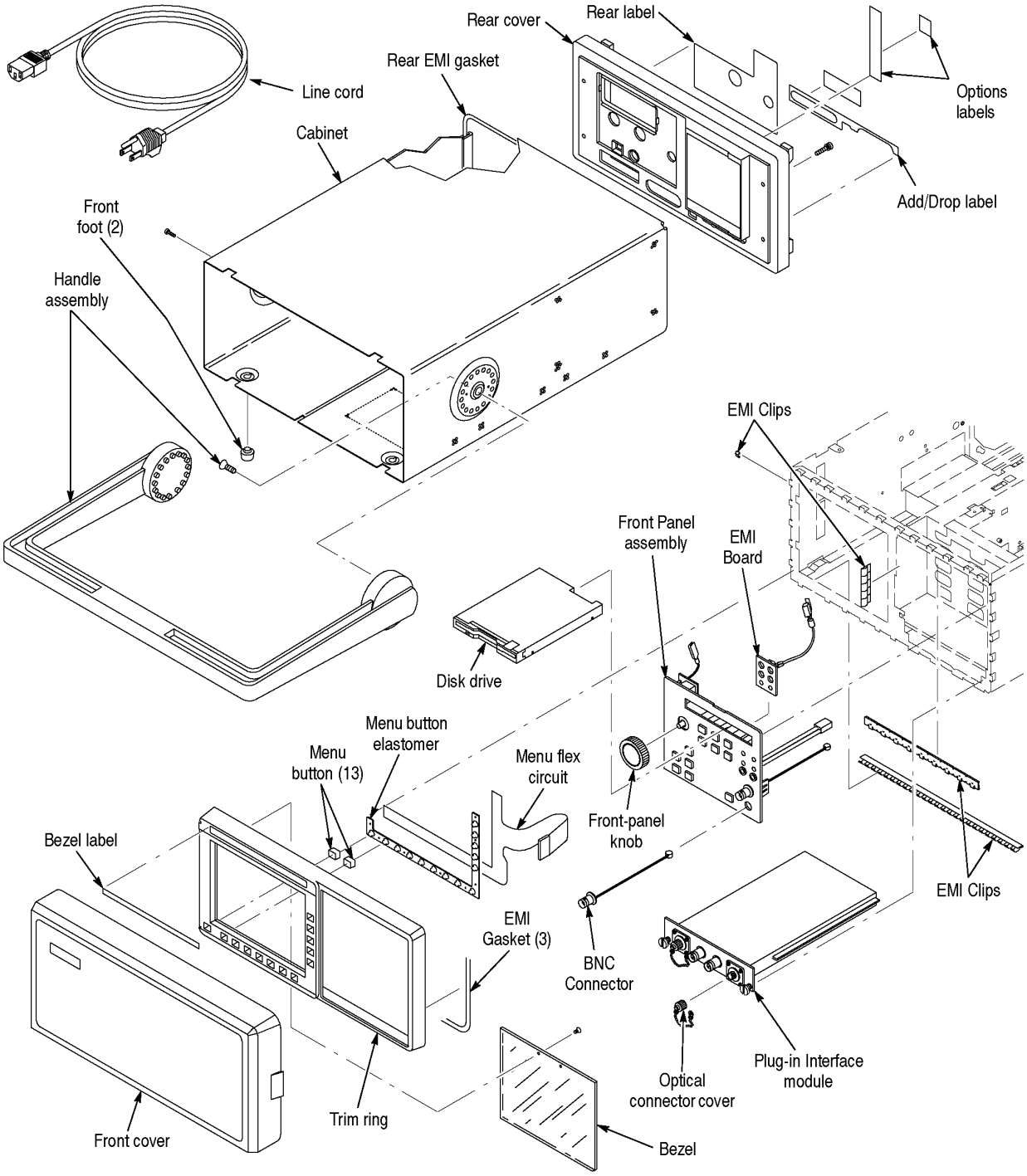


Figure 6-3: Cabinet and Front–Panel Mounted Modules

Table 6-5: Access Instructions for Modules in Figure 6-4

Procedure Including Module to be Removed	Page No.	Access Instructions
A10 Hi-Speed Protocol Assembly	6-37	1 Do the procedure listed at left to remove the module.
A09 Lo-Speed Protocol Assembly	6-38	1 Do *Com Bus, Board Supports, and PCAT Bus*, removing only the Com Bus and the PCAT Bus. 2 Do *Plug–In Interface Module*. 3 Do *A10 Hi-Speed Protocol Assembly*. 4 Do *Clock Generator to Lo-Speed Protocol.* 5 Do the procedure listed at left to remove the module.
A26 Monitor Assembly	6-39	1 Do the procedure listed at left, removing only the module(s) you want to service.
Com Bus, Board Supports, and PCAT Bus	6-42	1 Do the procedure listed at left to remove the module.
EMI Shield	6-43	1 Do the procedure listed at left to remove the module.
A01 Display/CPU Assembly	6-44	1 Do *EMI Shield*. 2 Do *Com Bus, Board Supports, and PCAT Bus*. 3 Do the procedure listed at left to remove the module.
A08 Clock Generator Assembly	6-46	1 Do *EMI Shield*. 2 Do *Com Bus, Board Supports, and PCAT Bus*. 3 Do *Clock Generator to Lo-Speed Protocol*. 4 Do the procedure listed at left to remove the module.
E1/E2/E3 Tributary and E4 Trib Assembly	6-47	1 Do *EMI Shield*. 2 Do *Com Bus, Board Supports, and PCAT Bus*. 3 Do the procedure listed at left to remove the module.
A12/A14 JAWA/JAWG Assembly	6-48	1 Do *EMI Shield*. 2 Do *Com Bus, Board Supports, and PCAT Bus*. 3 Do the procedure listed at left to remove the module.
A02 Backplane Assembly	6-50	1 Do *EMI Shield*. 2 Do *Com Bus, Board Supports, and PCAT Bus*. 3 Do the card–cage board procedures: *A03 CPU Assembly*, *A01 Display Assembly*, *A08 Clock Generator Assembly, E1/E2/E3 Tributary and E4 Trib Assembly,* and *JAWA/JAWG Assembly*. 4 Do the procedure listed at left to remove the module.

Table 6-5: Access Instructions for Modules in Figure 6-4 (continued)

Procedure Including Module to be Removed	Page No.	Access Instructions
Back–Up Battery	6-51	1 Do *EMI Shield*. 2 Do *Com Bus, Board Supports, and PCAT Bus*. 3 Do the card–cage board procedures: *A03 CPU Assembly*, *A01 Display Assembly*, *A08 Clock Generator Assembly*, *E1/E2/E3 Tributary and E4 Trib Assembly,* and *JAWA/JAWG Assembly*. 4 Do the procedure listed at left to remove the module.
Fan and Fan Mount	6-53	1 Do the procedure listed at left to remove the module.
A25 Low Voltage Power Supply and its Mount	6-55	1 *Only* if removing the plastic mount that secures the Low Voltage Power Supply, do all the procedures necessary to remove the *A02 Backplane Assembly*. 2 Do *Fan and Fan Mount*. Do not remove the fan mount. 3 Do the procedure listed at left to remove the module.
Line Filter	6-57	1 Do the procedure listed at left to remove the module.

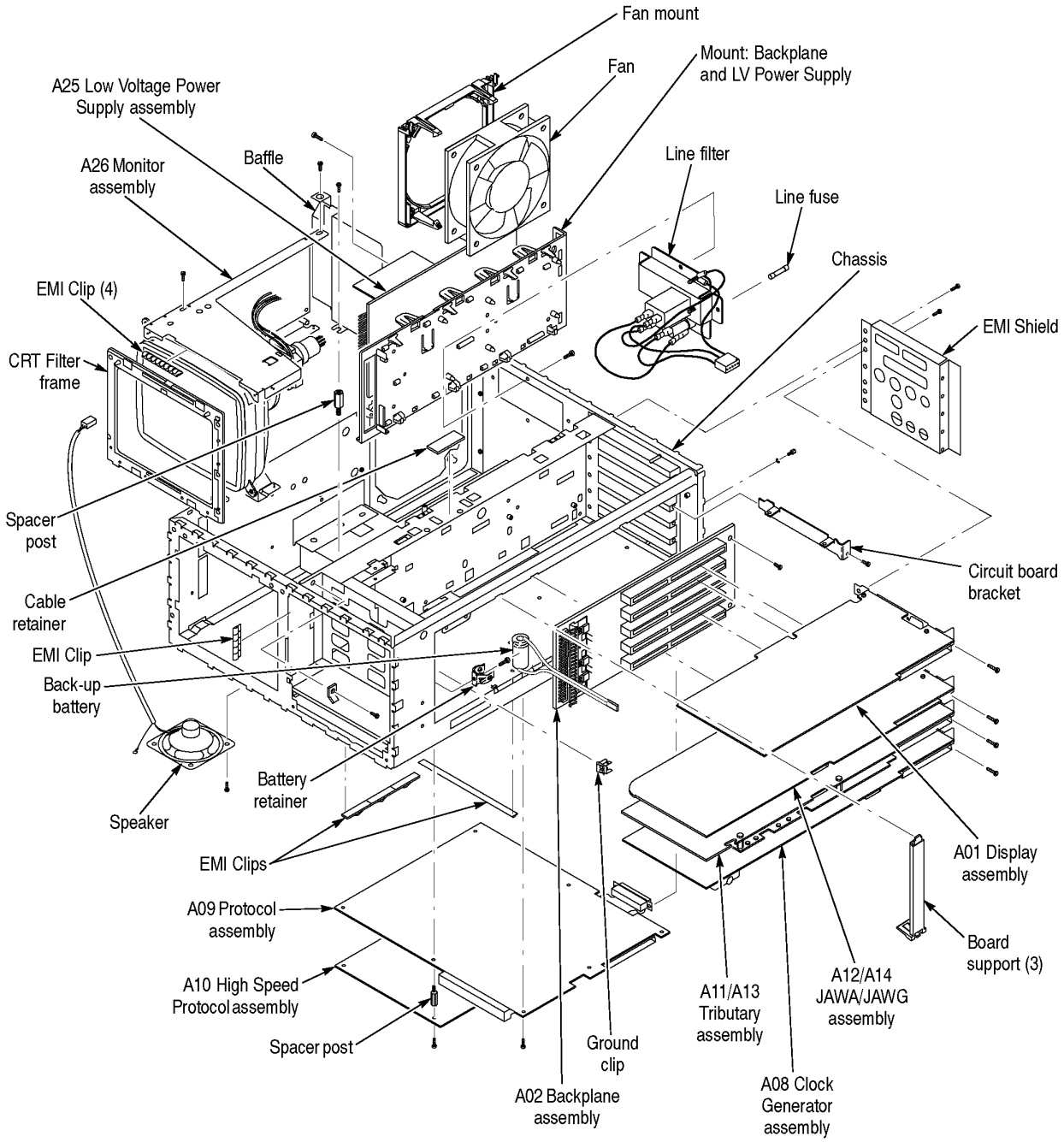


Figure 6-4: Internal Modules

Table 6-6: Access and Removal Instructions for Cables in Figures 6-5

Name of Cable	Access and Removal Instructions
Disk Drive–to–Display	1 Lift up on the latch at each side of both jacks. 2 Unplug the cable to be replaced from the disk drive and A03 CPU assemblies. 3 Reverse these instructions to install the replacement cable.
PCAT Bus	1 Unplug the cable to be replaced from the A01 Display and A09 Main Protocol assemblies. 2 Reverse these instructions to install the replacement cable.
Com Bus	1 Follow the procedure for removing the PCAT Bus. 2 Unplug the cable to be replaced from the board assemblies. 3 Reverse these instructions to install the replacement cable.
CPU–to–Front Panel	1 Find the procedure *A06 Front Panel Assembly and Menu Flex Circuit*. 2 Follow the access instructions found there to access and remove the A06 Front Panel assembly. The cables plugged into that assembly will be removed in the process. 3 Unplug the cable to be replaced from the A03 CPU assembly 4 Reverse these instructions to install the replacement cable.
Lo-Speed Protocol–to–Clock Generator	1 Find the procedure *Front Cover, Rear Cover, Cabinet, Rear EMI Gasket, and Cabinet Handle and Feet*. 2 Follow the access instructions found there to access and remove the rear panel and cabinet. 3 Unplug the Com Bus cable from the A09 Main Protocol and A08 Clock Generator assemblies. 4 Reverse these instructions to install the replacement cable.
Backplane–to–Low Voltage Power Supply–to–Main Protocol	1 Reach in from the top of the CTS 800–Series Test Set and unplug the cable at the jacks at the front of the backplane and Low–Voltage Power Supply modules. 2 Set the CTS 800–Series Test Set so its top is down. Unplug the cable to be replaced from the A09 Main Protocol assembly. 3 Reverse these instructions to install the replacement cable.
Auxiliary Power Supply–to–Line Filter *Auxiliary Power Supply–to–Low Voltage Power Supply*	1 Find the procedure *A07 Auxiliary Power Supply*. 2 Follow the access instructions found there to access and remove the Auxiliary Power Supply assembly. 3 Use a 15 W soldering iron to unsolder the cable from the Auxiliary Power Supply. 4 Reverse these instructions to install the replacement cable.
Auxiliary Power Supply–to–Low Voltage Power Supply–to–Ground Lug *Line Filter–to–Ground Lug*	1 If removing the Auxiliary Power Supply–to–Low–Voltage Power Supply–to–ground lug cable, unplug the cable from the Low–Voltage Power Supply and use a 15 W soldering iron to unsolder the cable from the Auxiliary Power Supply. 2 If removing the line filter–to–ground lug cable, unplug it from the line filter lug. 3 Using a 5/16 inch nut driver (Item 8) remove the nut(s) that secure the cable to be removed from the lug and remove it. 4 Reverse these instructions to install the replacement cable.

Monitor	1 Find the procedure *A01 Display Assembly*. 2 Follow the access instructions found there to access and remove the display assembly. The cable will be unplugged from that assembly in the process. 3 Unplug the cable from the monitor. 4 Unplug the cable from the Auxiliary Power Supply. 5 Reverse these instructions to install the replacement cable.

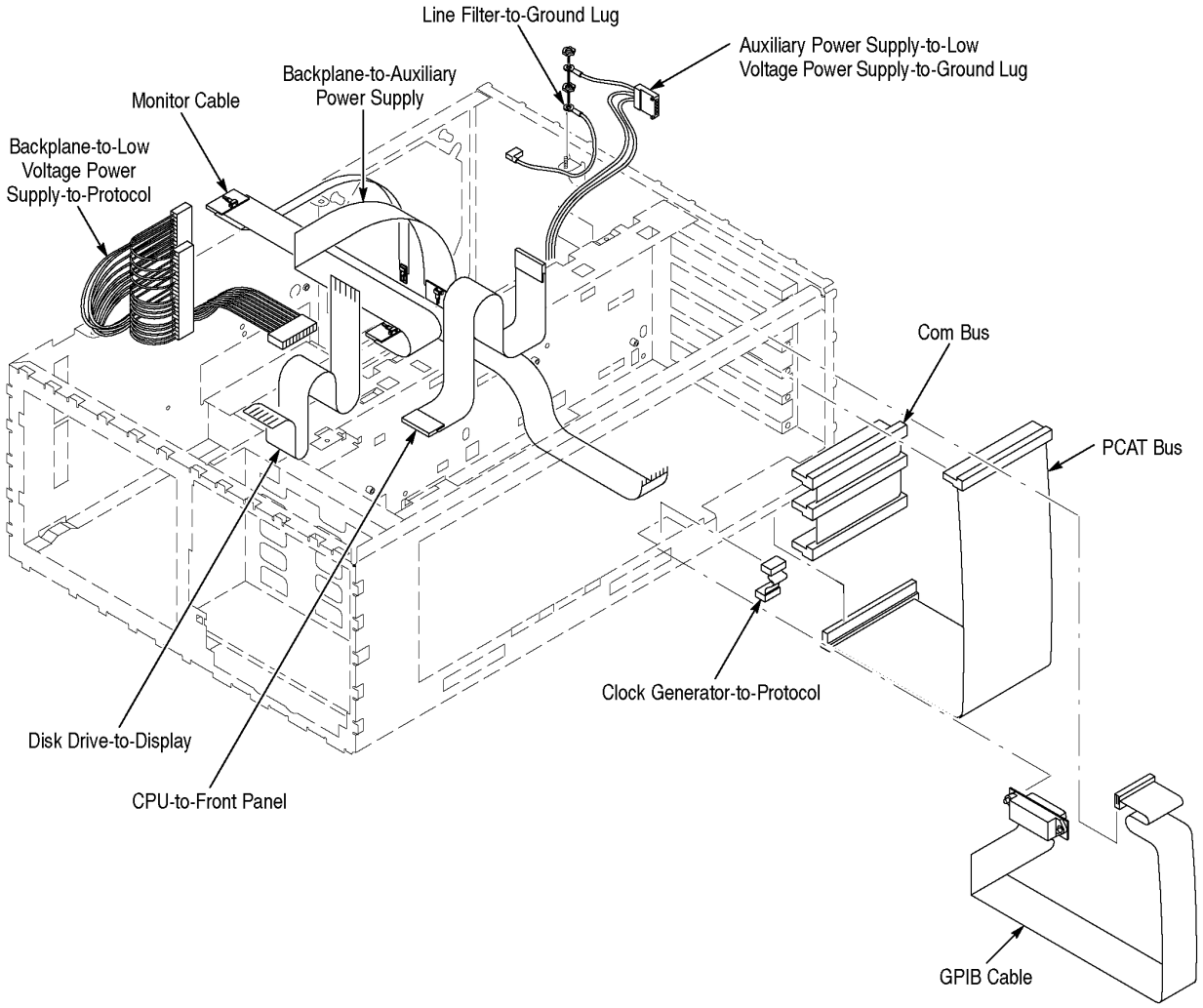


Figure 6-5: Cables and Cable Routing

Procedures for Module Removal and Installation

Do the *Access Procedure* before doing any procedure in this collection.

Optical Port Connection

The CTS is shipped with the FC connector bulkhead and dustcap installed. If you wish to replace the connector or change to the ST, DIN 47256, or SC connectors perform the following procedure:

1. Verify that the CTS has been turned off with the principal power switch on the rear panel and that the power cord has been removed.
2. Remove the four screws that attach the bulkhead connector to the front panel.
3. Gently pull the bulkhead out of the unit and unscrew the fiber connector. Be careful not to pull beyond the fiber slack.
4. Disassemble the bulkhead as shown in Figures 6-6 through 6-9.

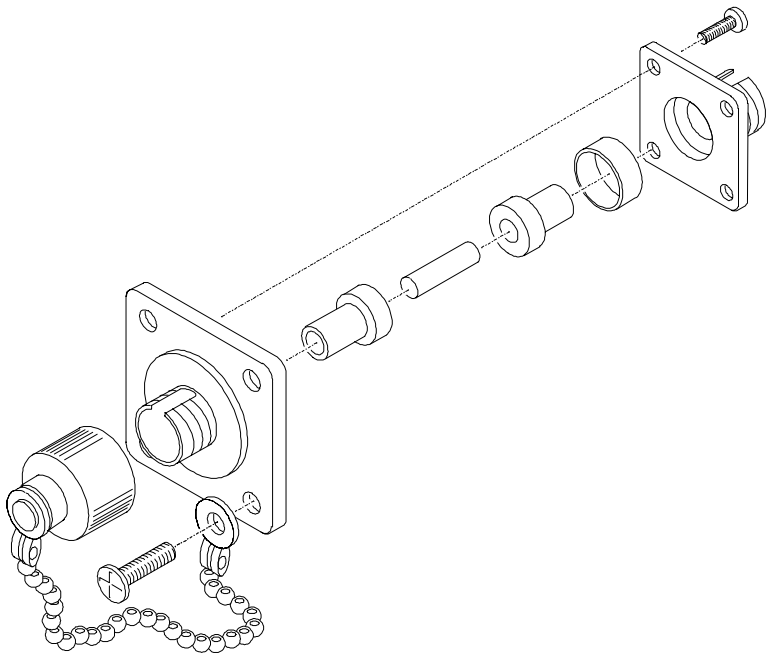


Figure 6-6: FC Optical Bulkhead Assembly

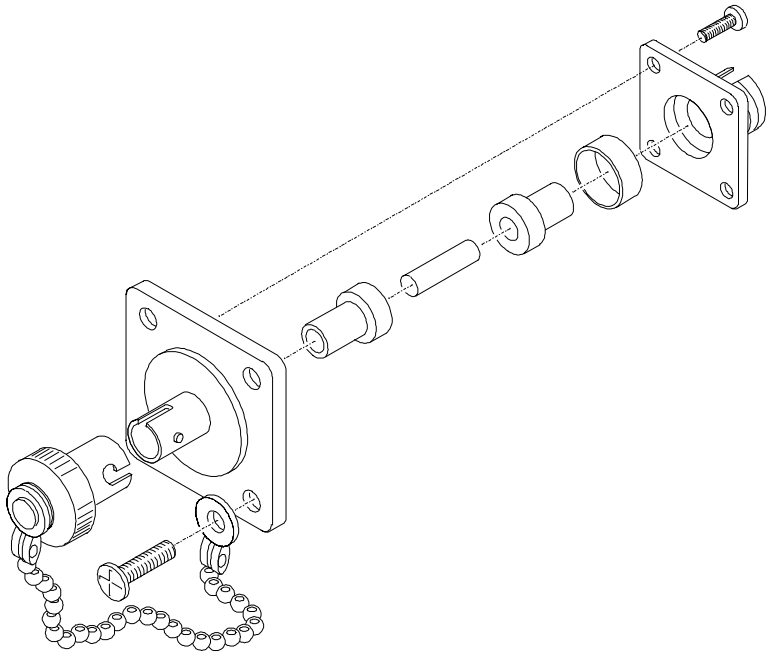


Figure 6-7: ST Optical Bulkhead Assembly

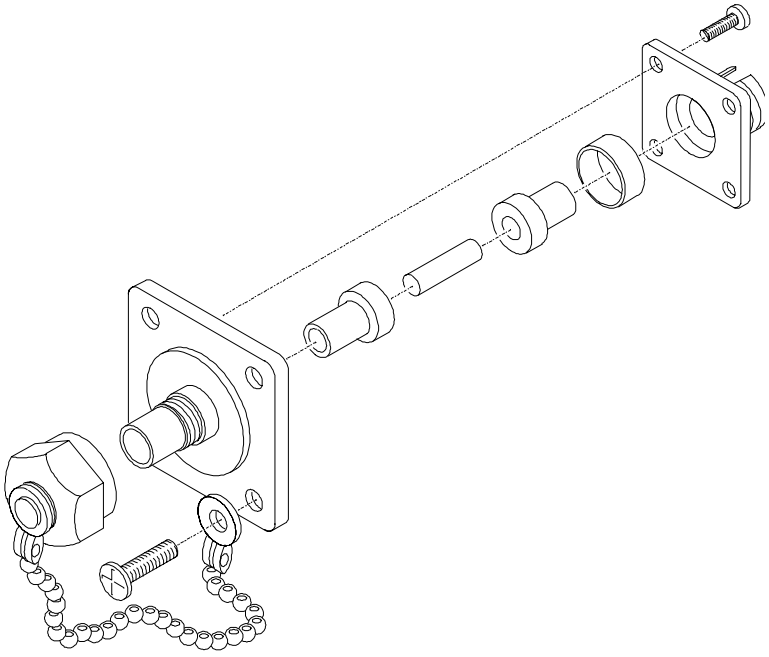


Figure 6-8: DIN 47256 Optical Bulkhead Assembly

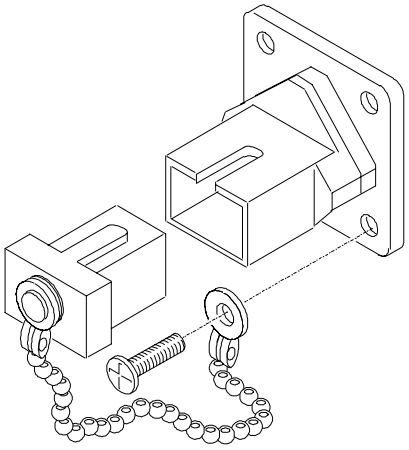


Figure 6-9: SC Optical Bulkhead Assembly

5. Replace the current bulkhead with the one you wish to use and re–assemble.
6. The final part of installation is the reverse of steps 1 through 3.

Front-Panel Knob

For this procedure you will need a 1/16 inch hex key screwdriver (item 12).

1. Set the CTS so its bottom is down on the work surface and its front is facing you.
2. To remove the knob, loosen the Allen screw in the side of the knob (see Figure 6-10).
3. To reinstall, hold the knob in place and tighten the Allen screw. Be sure the knob is not scraping against the front panel.

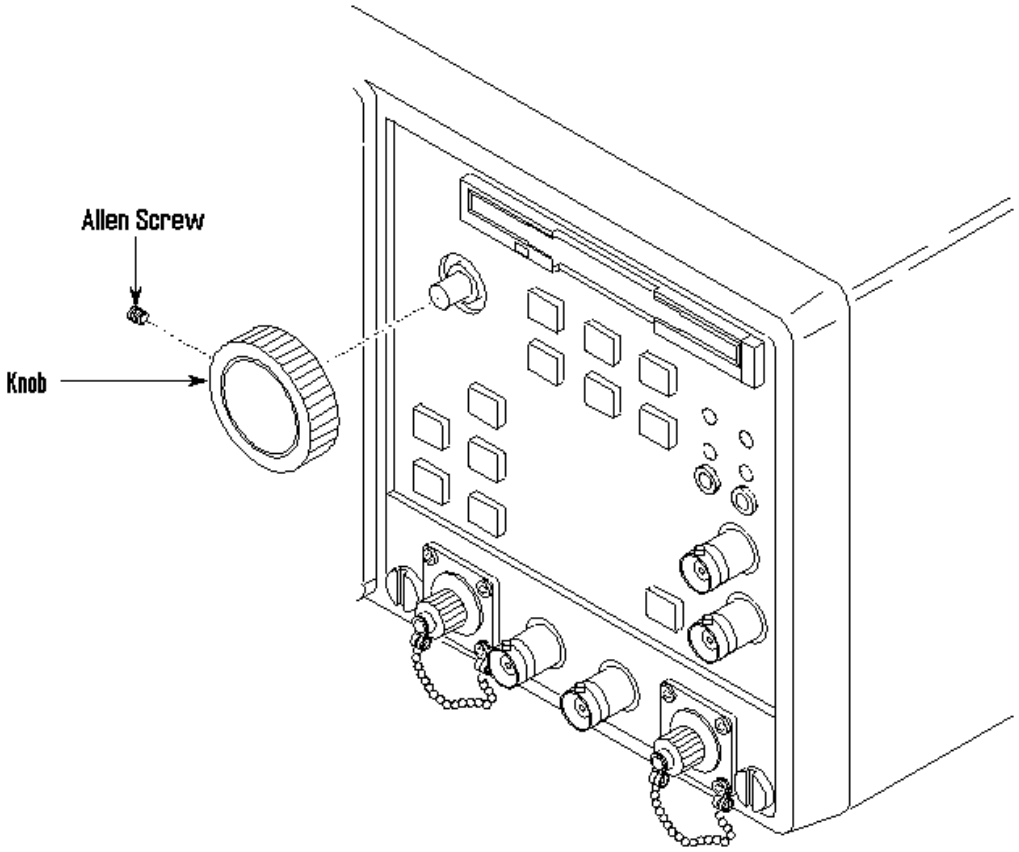


Figure 6-10: Knob Removal

Line Fuse

For this procedure you will need a flat–bladed screwdriver.

WARNING: Unplug the line cord from the line voltage power source before continuing. Failure to do so can cause death or injury.

1. Locate the line fuse in Figure 6-11.
2. Set the CTS so its bottom is down on the work surface and its rear is facing you.

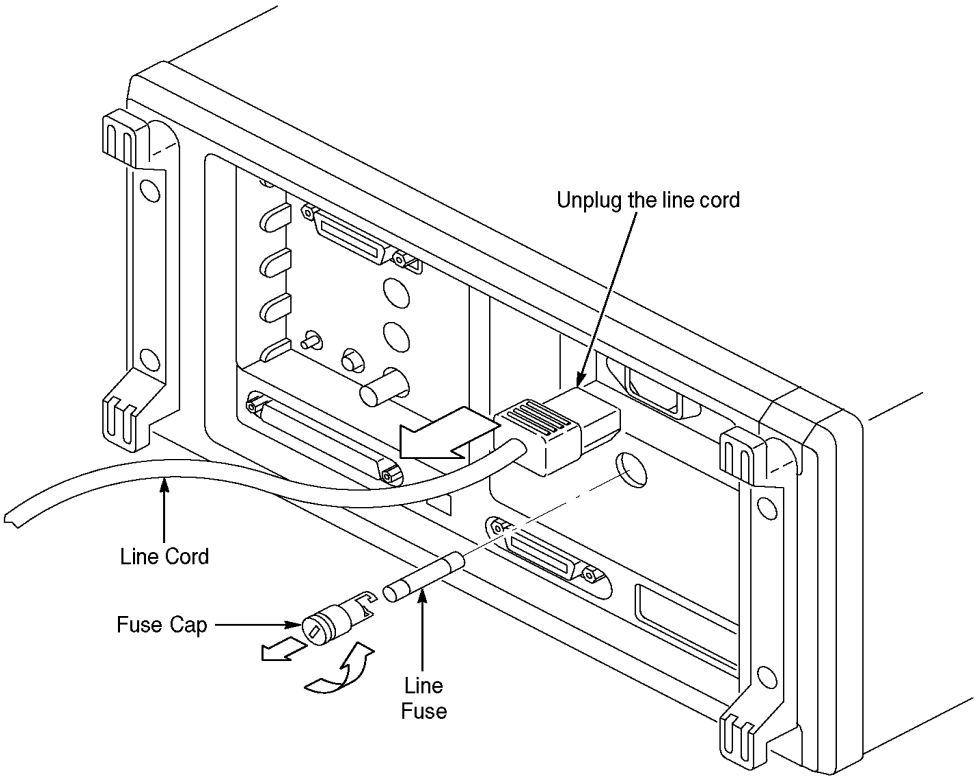


Figure 6-11: Line Fuse

3. To remove the line fuse, turn the fuse cap counterclockwise using a flat–bladed screwdriver.
4. To reinstall the line fuse, do step 3 in reverse.

Rear Cover, Cabinet, Front and Rear EMI Gaskets, Cabinet Handle and Feet

For this procedure you will need a screwdriver with size T–15 and T–20 TorxR tips and a flat–bladed screwdriver. If removing the EMI gasket, you will also need a pair of needle–nose pliers.

1. Make sure the CTS front cover is installed; if not, install it by snapping its edges over the trim ring.
2. Rotate the handle toward the bottom of the CTS, and then set the CTS front down on the work surface with the bottom facing you (see Figure 6-12).
3. If removing a front foot for replacement, use a pair of slip–jaw pliers to firmly grip the foot, and then pull with a turning motion to remove. Reverse the process to install the replacement foot.
4. To remove the rear cover, remove the four T–15 Torx–drive screws securing the rear cover to the CTS. Lift off the rear cover. If no other modules are being serviced, skip to the end (step 10) of this procedure.
5. If removing a rear foot for replacement, use a flat–bladed screwdriver to press the foot out from inside the rear cover. Use your hand to press a replacement foot into the rear cover. If no other modules are being serviced, skip to the end (step 10) of this procedure.
6. If removing the EMI shield from the rear cover, remove the Torx-drive screws and then remove the shield. If no other modules are being serviced, skip to the end (step 10) of this procedure.

NOTE: *DO NOT do step 9 to remove the EMI gasket from the rear of the cabinet unless it must be replaced due to damage. If you are not replacing that gasket, skip to step 10.*

When reinstalling the EMI gasket and the CTS cabinet, carefully follow the instructions given. Unless they are performed properly, the CTS may not meet its emissions requirements (EMI).

7. To remove the cabinet, perform the following steps:
   - **a.** Remove the single T-15 Torx–drive screw at the left side of the CTS.
   - **b.** Grasp the two handle hubs and pull them outward as if to rotate the handle.
   - **c.** While holding the handle hubs pulled out, lift the cabinet upward to slide the cabinet off the CTS.
   - **d.** At the rear of the cabinet, grasp its left and right edges. Take care not to bind or snag the cabinet on the internal cabling as you remove the cabinet.

e. If no other cabinet modules are being serviced, skip the end (step 10) of this procedure.

NOTE: *DO NOT do step 9 to remove the EMI gasket from the rear of the cabinet unless it must be replaced due to damage. If you are not replacing that gasket, skip to step 10.*

When reinstalling the EMI gasket and the CTS cabinet, carefully follow the instructions given. Unless they are performed properly, the CTS may not meet its emissions requirements (EMI).

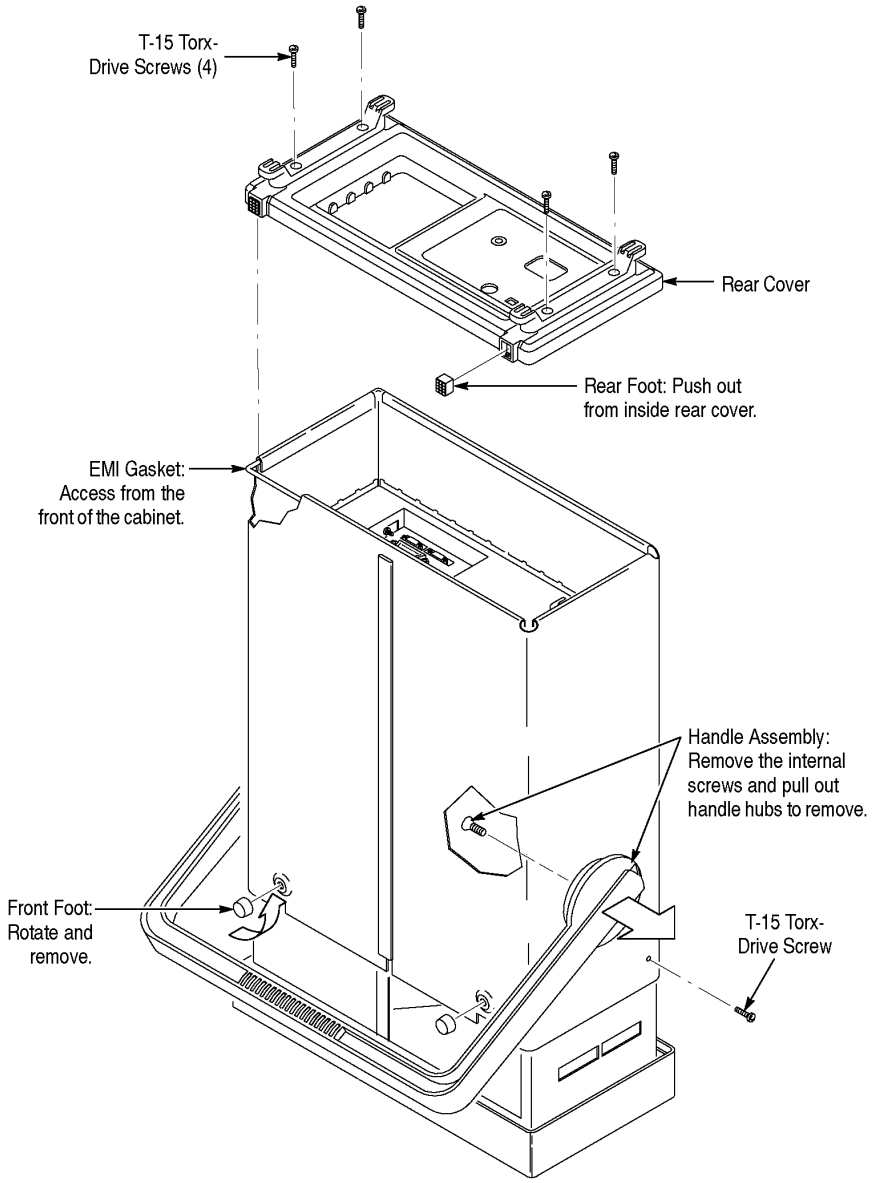


Figure 6-12: Front & Rear Covers, Cabinet, EMI Gasket, Handle, & Feet Removal

8. If removing the handle assembly for cleaning or replacement, perform the following steps:

a. Working from the inside of the cabinet, remove the T–20 Torx–drive screw securing each handle hub to the cabinet.

b. Working from the outside of the cabinet, grasp the two handle hubs and pull them outward from the cabinet until they are out of the cabinet.

c. While holding the handle hubs pulled out, lift the handle away to remove.

NOTE: *DO NOT do step 9 to remove the EMI gasket from the rear of the cabinet unless it must be replaced due to damage. If you are not replacing the gasket, skip to step 10.*

When reinstalling the EMI gasket and the CTS cabinet, carefully follow the instructions given. Unless they are performed properly, the CTS may not meet its emissions requirements (EMI).

9. If removing the EMI gasket for replacement, perform the following steps:

a. Locate the EMI gasket to be removed in the diagram *Front Cover, Rear Cover, Cabinet, EMI Gasket, and Cabinet Handle and Feet Removal*.

b. Look for the point where the ends of the gasket touch in the channel at the rear edge of the cabinet.

c. Use a pair of needle–nose pliers to pry up one of the ends of the gasket.

d. Grasp the EMI gasket, and gently pull it out of its channel.

10. To reinstall the cabinet and rear cover, perform the following steps:

a. If the EMI gasket was removed, press the new EMI gasket into its groove at the rear edge of the cabinet. Make sure the ends of the gasket touch, but do not overlap. (Cut off excess length if required to prevent overlap.)

b. See step 8 to reinstall the handle assembly (if it was removed).

c. Do step 6 in reverse order to reinstall the cabinet, while observing the following precautions and requirements:

- Take care not to bind or snag the cabinet on internal cabling; dress cables as necessary.
- When sliding the cabinet onto the CTS, be sure the ridge around the rear of the main chassis slides into the groove containing the EMI gasket on the rear of the cabinet.
- Install the four screws at the rear panel, and tighten to 8 inch–lbs torque before installing the single screw at the left side of the cabinet. Tighten this screw to 8 inch–lbs.

d. See step 5 to reinstall the rear cover. If installing a new rear cover, also do the following:

- Find the appropriate labels for your rear cover.
- Remove the covering from the back of the sticky–back label, align it to the rear cover, and press firmly to install.

Trim Ring, Menu Elastomer, Menu Buttons, and Front EMI Gaskets

For this procedure you will need a spudger.

1. Set the CTS so its rear is down on the work surface and its bottom is facing you (see Figure 6-13).

2. If the front cover is installed, remove it by grasping its left and right edges and snapping it off the front of the CTS.

WARNING. Do not touch the carbon contact points on the menu elastomer installed in the trim ring. Also, do not touch the contacts on the menu button flex circuit exposed when you remove the trim ring. You should wear clean cloth gloves that are free of lint when handling the menu elastomer or when touching the menu button flex circuit mounted on the front chassis.

3. To remove the trim ring, pull the top flex locks outward, and then lift the top of the trim ring forward to snap it loose from the main chassis. Repeat the process to loosen the bottom edge of the trim ring. When removed, lay the trim ring on its face on the work surface.

4. To remove the front EMI gaskets, lift them out of the trim ring.

5. If servicing the menu elastomer, lift it out of the trim ring.

6. If servicing the menu buttons, lift them out of the trim ring.

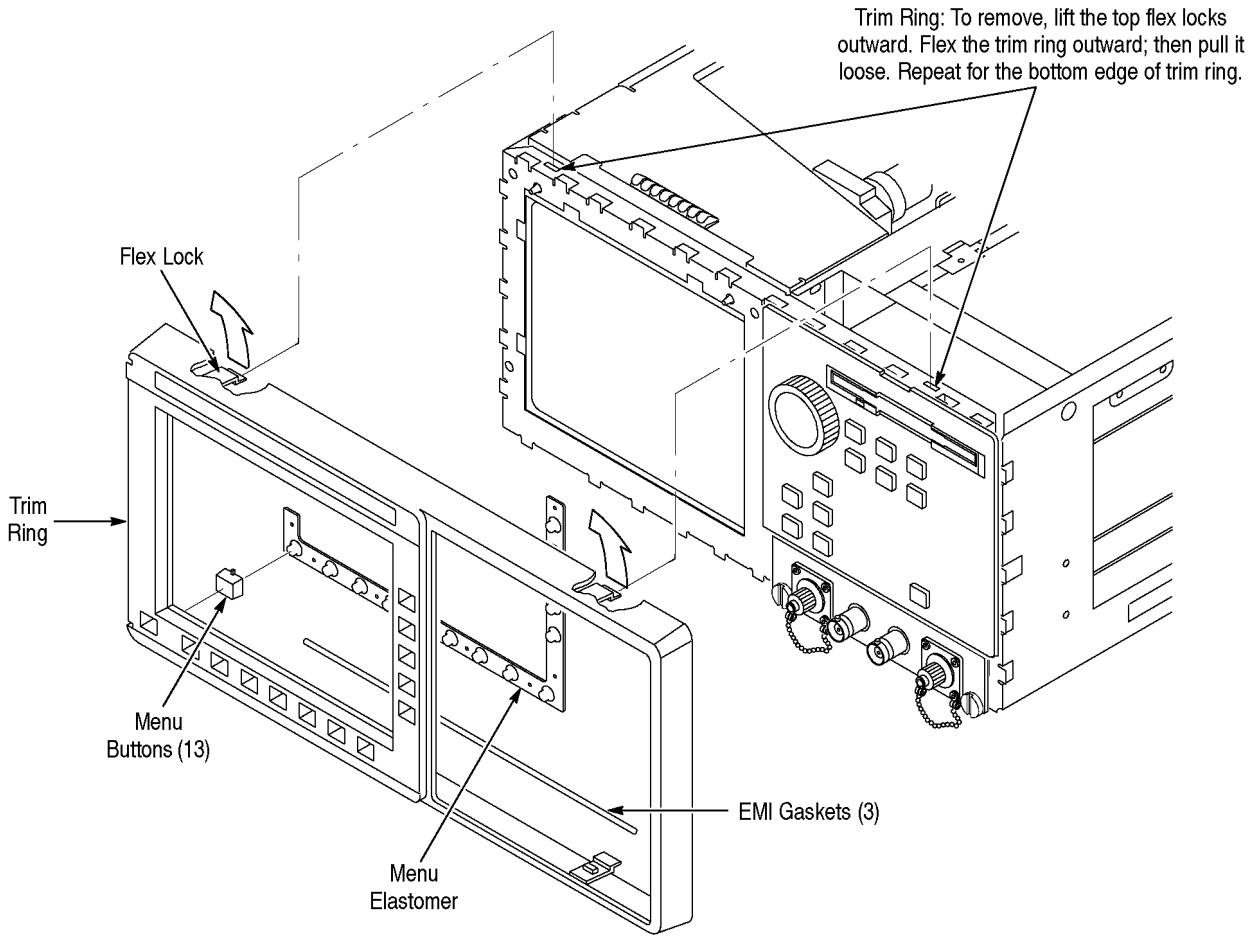


Figure 6-13: Trim Ring, Menu Elastomer, and Menu Buttons Removal

7. To reinstall the trim ring, perform the following steps:

a. If the menu buttons were removed, insert each button into its hole in the trim ring.

b. If the menu elastomer was removed, align it over the menu button holes in the trim ring, and press it in to install. Avoid touching the carbon contact points on the elastomer when installing.

c. Without installing the EMI gaskets, align the trim ring to the front of the chassis, and push it on to seat. Be sure that both pairs of flex locks, one pair each at the inside top and bottom of the trim ring, snap over the edge of the chassis.

8. To reinstall the EMI gaskets, perform the following steps (see Figure 6-14):

a. Install the front cover on the CTS.

b. Lay the CTS so its front cover is on the work surface.

c. Align an EMI gasket so it lays in the groove between the trim ring and the chassis between the top pair of flex locks.

d. Using a spudger, push the EMI gasket until it is firmly seated at the bottom of the groove. It should not overlap either flex lock.

e. Repeat the process just described to install the remaining two side gaskets.

9. If the trim ring installed in step 7 is a new trim ring, also do the following:

a. Find the label that matches your model CTS.

b. Remove the covering from the back of the sticky–back label, align it to the trim ring, and press firmly to install.

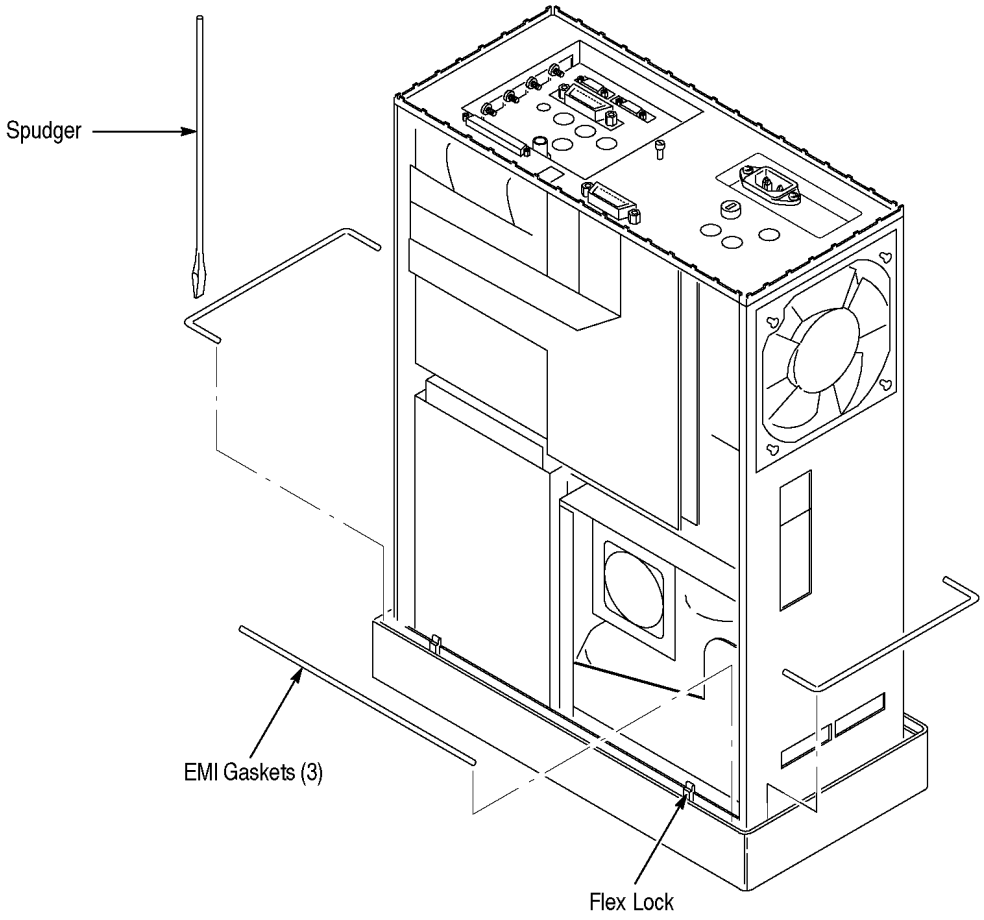


Figure 6-14: EMI Gasket Installation

Plug-In Interface Module

For this procedure you will need a flat–bladed screwdriver.

1. Set the CTS so its bottom is down and its front is facing you.

2. To remove the Plug–In Interface Module, perform the following steps using Figure 6-15 as a guide:

   a. If not already installed, screw the dust caps onto the optical connectors.

   b. Using a screwdriver, loosen the two screws on the front panel of the module.

   c. Grasp the module by its two front–panel screws, and slide the module out of the front panel to complete its removal.

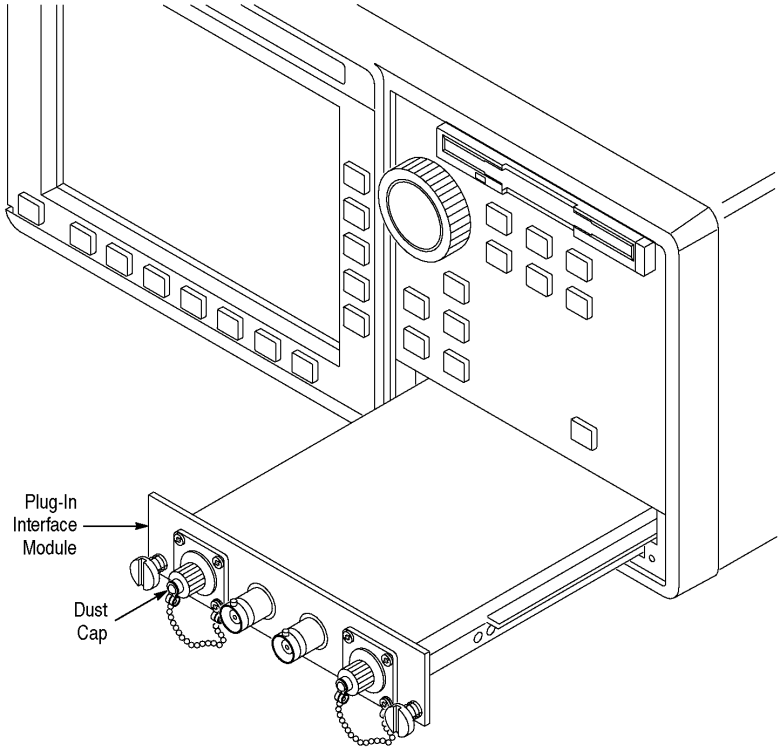


Figure 6-15: Plug-in Interface Module Removal

3. To reinstall the Plug–In Interface Module, perform the following steps:

    a. Align the Plug–In Interface module edges with the guides, and then slide it into the cavity of the CTS.

    b. Using both thumbs, press on the Plug–In Interface Module front panel until the module is completely seated in the CTS.

    c. With the screwdriver, tighten each thumbscrew until snug.

Disk Drive

For this procedure you will need a screwdriver with a size T–15 Torx tip and a Pozidriv screwdriver.

1. If you have not already performed the *Access Procedure* and removed the modules as instructed, do so now.

2. Set the CTS so its bottom is down and its front is facing you.

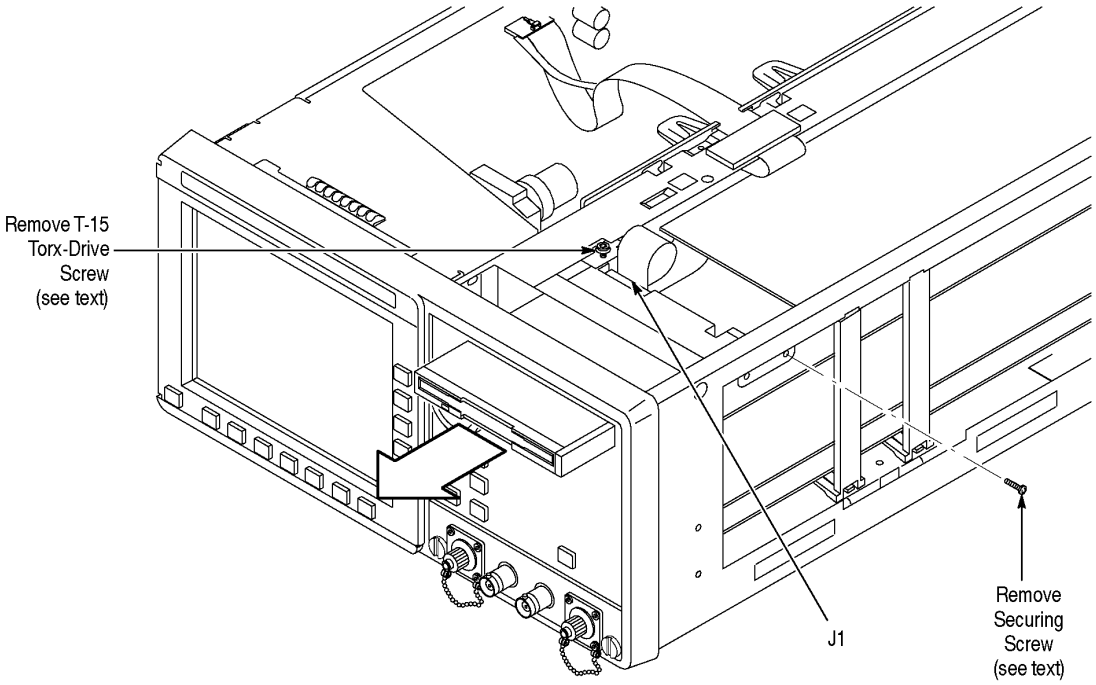


Figure 6-16: Disk Drive Removal

3. To remove the disk drive, perform the following steps using Figure 6-16 as a guide:

    a. Lift up on the two locking tabs on J1 of the disk drive.

    b. Remove the cable from the drive.

    c. If present, remove the T–15 Torx–drive screw that clamps the drive in the chassis. When replacing the drive, do not reinstall this screw.

    d. Remove the one or two screws securing the drive to the chassis.

    e. Grasp the drive by its front edges, and pull it out of the front panel to complete its removal.

    f. If present, remove the screw securing the spacer to the drive, and lift the spacer away from the drive to complete the removal.

4. To reinstall the disk drive, perform steps 3a-3f in reverse order.

A06 Front Panel Assembly and Menu Flex Circuit

For this procedure you will need a flat–bladed screwdriver and hex key screwdriver .

1. If you have not already performed the *Access Procedure* and removed the modules as instructed, do so now.

2. Set the CTS so its bottom is down on the work surface and its front is facing you.

3. To remove the A06 Front Panel assembly, perform the following steps using Figure 6-17 as a guide:

    a. If your CTS contains the optional Add/Drop/Test connectors, unplug the following cables (your CTS may not contain all three cables) from their jacks on the Tributary assembly (J225, J217, J218, and J220 on Option 22; J225, J5, J6, and J7 on Option 36).

    b. Insert a flat–bladed screwdriver into the slot at the front right of the chassis. Push inwards to release the snap lock at the right side.

    c. While guiding the Add/Drop cables, if any, through the chassis access holes, lift the A06 Front Panel assembly out of the front of the main chassis until you can reach the interconnect cables connecting it to various other modules.

d. Unplug the following cables from their jacks on the A06 Front Panel assembly:

- The CPU–to–front–panel cable at J101
- The menu flex circuit at J301
- The ground cable to chassis ground lug

e. Finally, lift the A06 Front Panel assembly out of the front of the main chassis to complete the removal.

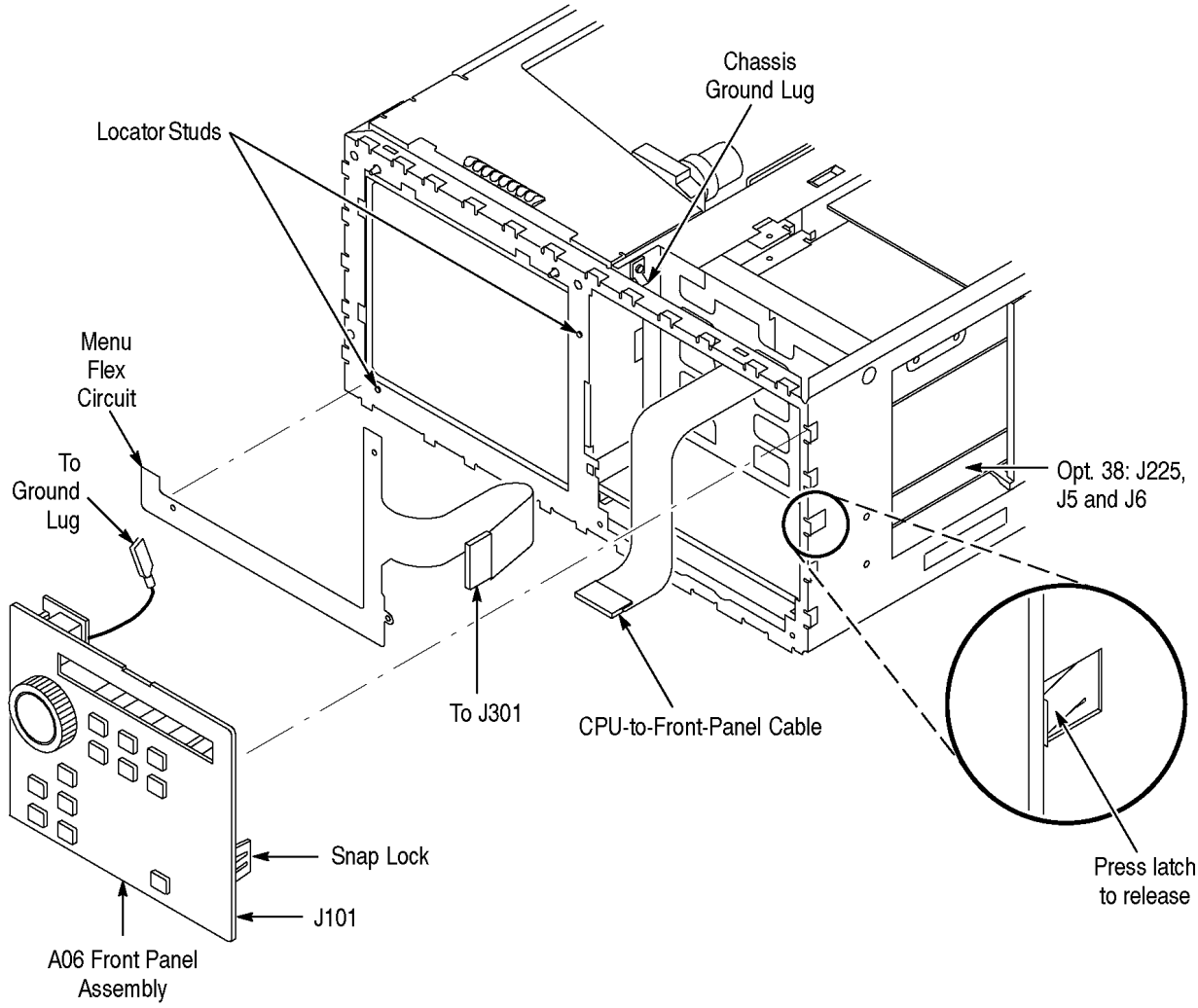


Figure 6-17: A06 Front Panel Assembly and Menu Flex Circuit Removal

NOTE: *Perform step 4 only if disassembling for cleaning and lubrication. (Components removed in step 4 are not field replaceable.) Otherwise, skip to step 5 to continue this procedure.*

4. If the front panel or the front–panel buttons are to be cleaned, perform the following steps:

    a. Remove the knob from the A06 Front Panel assembly using the method described in *Front–Panel Knob* .

    b. Release the four snap locks at the edge of the circuit board and the snap lock near the center of the circuit board, and then lift the board away from the assembly (see Figure 6-18).

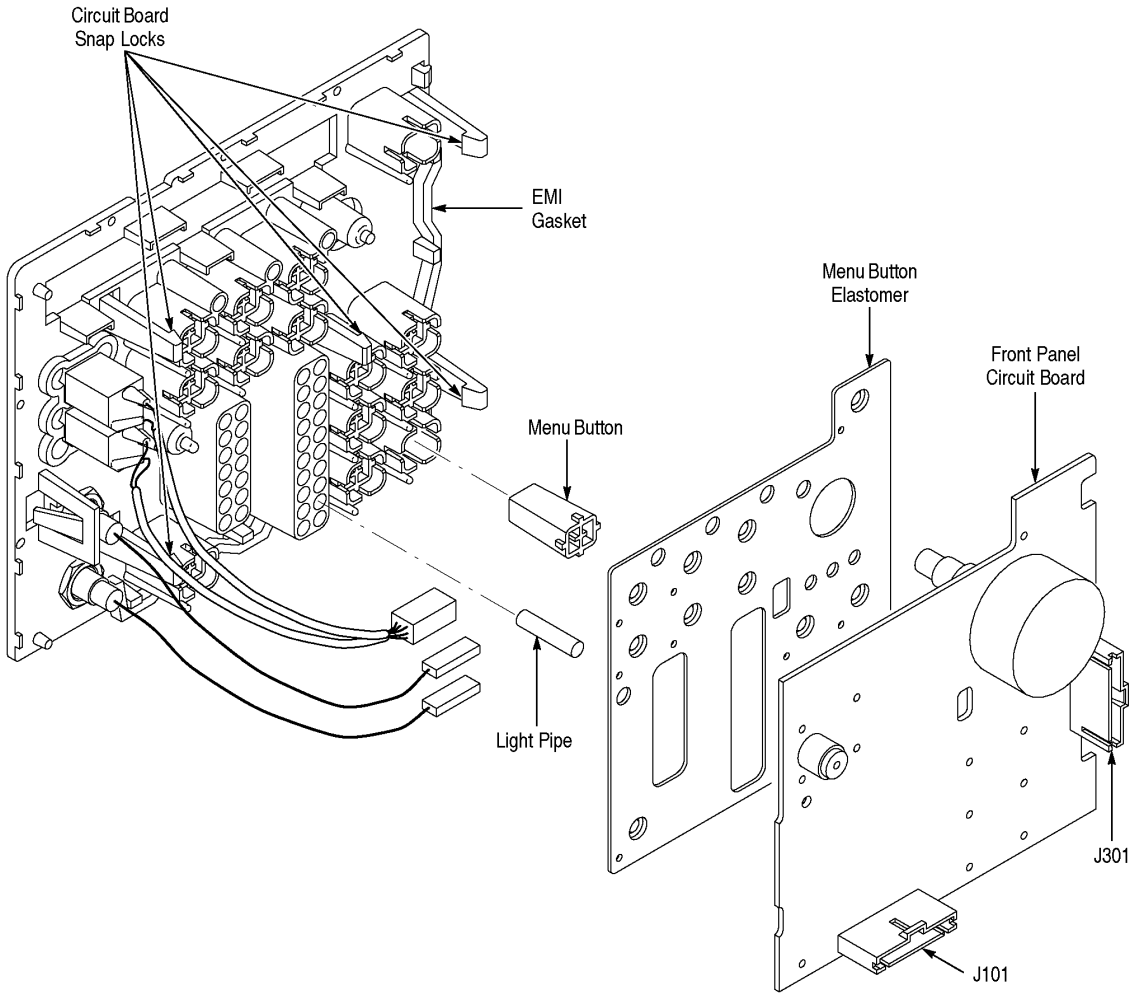


Figure 6-18: Disassembly of the Front Panel Assembly

c. Disassemble the front–panel–assembly components using Figure 6-18 as a guide. During disassembly, be careful not to spill the light pipes from their sockets; the light pipes are not attached and can slide out easily.

d. Reverse the procedure to reassemble.

CAUTION: *Perform step 5 only if replacing a failed or damaged menu flex circuit with a new unit from the factory. (Removal of the circuit is likely to destroy it.) If this is not the case, skip to step 7 to continue this procedure.*

5. To remove the menu flex circuit, perform the following steps:

a. Slowly pull the flex circuit away from the front of the main chassis. (Removing the flex circuit slowly helps keep the adhesive backing from sticking to the chassis.)

b. Wipe the front of the chassis using isopropyl alcohol and a clean, lint–free cloth. Make sure to remove any adhesive left over from the old flex circuit. Let dry.

6. To install a new menu flex circuit, perform the following steps:

a. Do not touch the contacts on the menu flex circuit with your bare fingers. You should wear clean cloth gloves that are free of lint when installing the menu flex circuit on the front chassis.

b. Find the score line in the adhesive backing and peel the backing off the menu flex circuit.

c. Carefully align the three holes on the menu flex circuit to the locator studs on the front of the main chassis. (See Figure 6-3.) When the alignment is correct, press the flex circuit against the chassis so it adheres to the chassis.

d. Clean the surface of the menu flex circuit just installed using isopropyl alcohol and a clean, lint–free cloth.

7. To reinstall the A06 Front Panel assembly, perform steps 3a-3d in reverse order. Be sure to dress the CPU–to–front–panel cable so that the loop of extra cable length is in the front–panel cavity of the chassis.

A10 High Speed Protocol Assembly

For this procedure you will need a screwdriver with a size T–15 Torx tip.

1. If you have not already performed the *Access Procedure* and removed the modules as instructed, do so now.
2. Set the CTS so its top is down and its left side is facing you.
3. To remove the A10 High Speed Protocol board, perform the following steps using Figure 6-19 as a guide:
   a. Remove four T–15 Torx–drive screws securing the board to chassis.
   b. Grasp the board by its edges, and pull upward to unplug it from the A09 Main Protocol assembly.
   c. Lift the board away from the chassis to complete its removal.
4. To reinstall the A10 High Speed Protocol board, perform steps 3a-3c in reverse order.

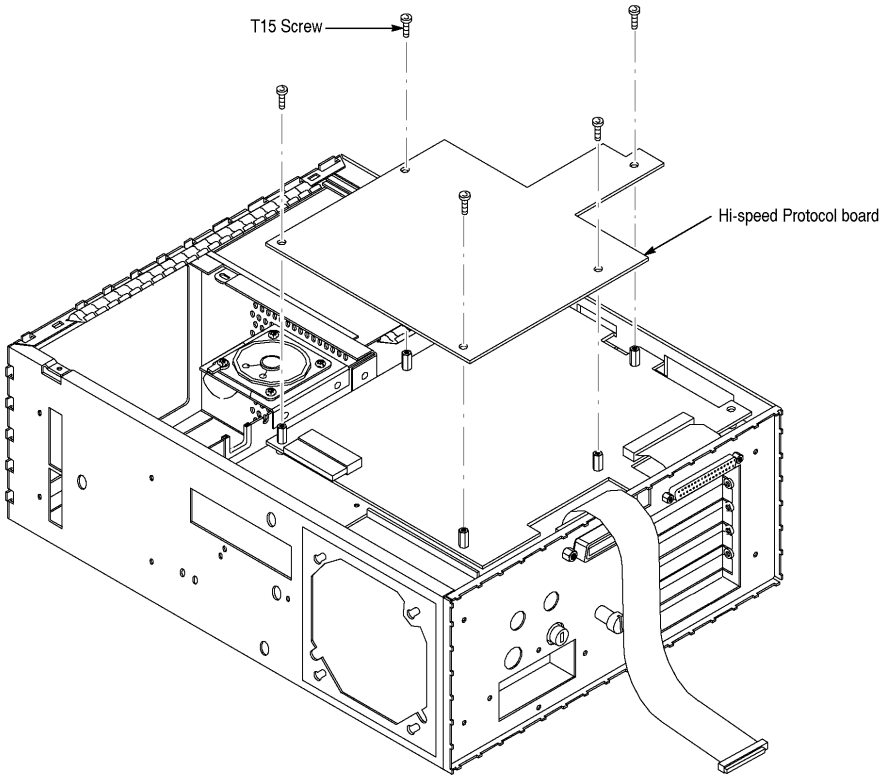


Figure 6-19: A10 Hi-Speed Protocol Assembly Removal

A09 Lo-Speed Protocol Assembly

For this procedure you will need a screwdriver with a size T–15 Torx tip and 3/16 inch and 1/4 inch nut drivers.

1. If you have not already performed the *Access Procedure* and removed the modules as instructed, do so now.
2. Set the CTS so its right side is up, with its bottom facing you.
3. To remove the A09 Lo-Speed Protocol assembly, perform the following steps using Figure 6-20 as a guide:
    a. Unplug the cable from the low voltage power supply assembly from J15.
    b. Unplug the cable from the A08 Clock Generator assembly from J930.
    c. Remove the two 3/16 inch screws securing the Overhead Add/Drop connector to the rear panel.
    d. Remove the four 1/4 inch spacer posts securing the A09 Lo-Speed Protocol assembly to the bottom of the chassis.
    e. Remove the three T–15 Torx–drive screws securing the A09 Lo-Speed Protocol assembly to the bottom of the chassis, and lift out the A09 Main Protocol assembly to complete its removal.
4. To reinstall the A09 Lo-Speed Protocol assembly, perform steps 3a-3e in reverse order.

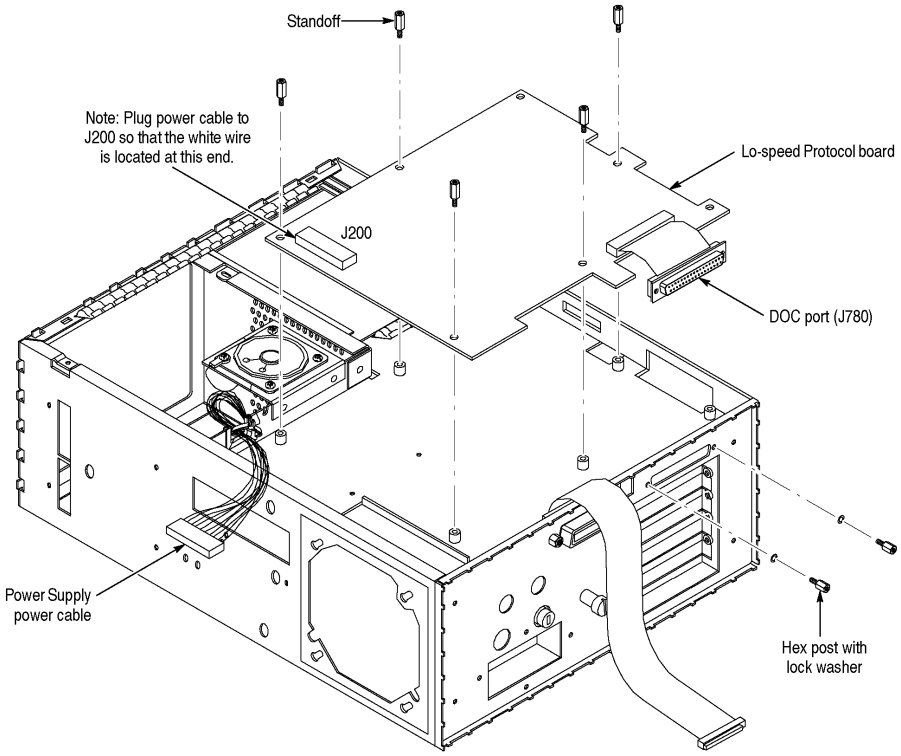


Figure 6-20: A09 Lo-Speed Protocol Assembly Removal

A26 Monitor Assembly

For this procedure you will need a screwdriver with a size T–15 Torx tip.

1. If you have not already performed the *Access Procedure* and removed the modules as instructed, do so now.

NOTE: *The display tube and the display–driver board are a single module and must be removed and replaced as one unit. They are listed as a single module in the Mechanical Parts List.*

2. Set the CTS so its bottom is down on the work surface, with its front facing you.

WARNING: Use care when handling a monitor. If you break its display tube it may implode, scattering glass fragments with high velocity and possibly injuring you. Wear protective clothing, including safety glasses (preferably a full–face shield). Avoid striking the display tube with or against any object.

Store the monitor with its display tube face down in a protected location, placing it on a soft, nonabrasive surface to prevent scratching the face plate.

3. To remove the monitor, perform the following steps using Figure 6-21 as a guide:

a. Unplug the main cable at (J901), and then rotate the CTS so its top is down on the work surface, with its bottom facing upwards.

b. Remove the three T–15 Torx–drive screws securing the monitor assembly to the bottom of the main chassis. Return the CTS to the orientation established in step 2.

WARNING: *High voltage is present on the anode lead. It is not necessary to unplug the anode from the monitor when removing or replacing the monitor module; therefore, do not do so.*

c. Remove the three T–15 Torx–drive screws securing the monitor assembly to the top of the chassis. (See Figure 6-7 to locate the screws.)

d. Lift the left top flex lock on the trim ring, and pull the left corner of the trim ring forward slightly.

e. Tilt the rear of the monitor assembly upward slightly. Slide the monitor assembly back in the main chassis until it stops (about 3/4 inch). Now lift it straight up out of the top of the main chassis to complete the removal.

f. Store the monitor assembly in a protected location. Place it face down on a soft, nonabrasive surface to prevent scratching the face plate.

g. If replacing the CRT filter frame, press the locking tab at the top center of the frame while pushing the frame into the CTS. Lift the frame out of the chassis to complete its removal.

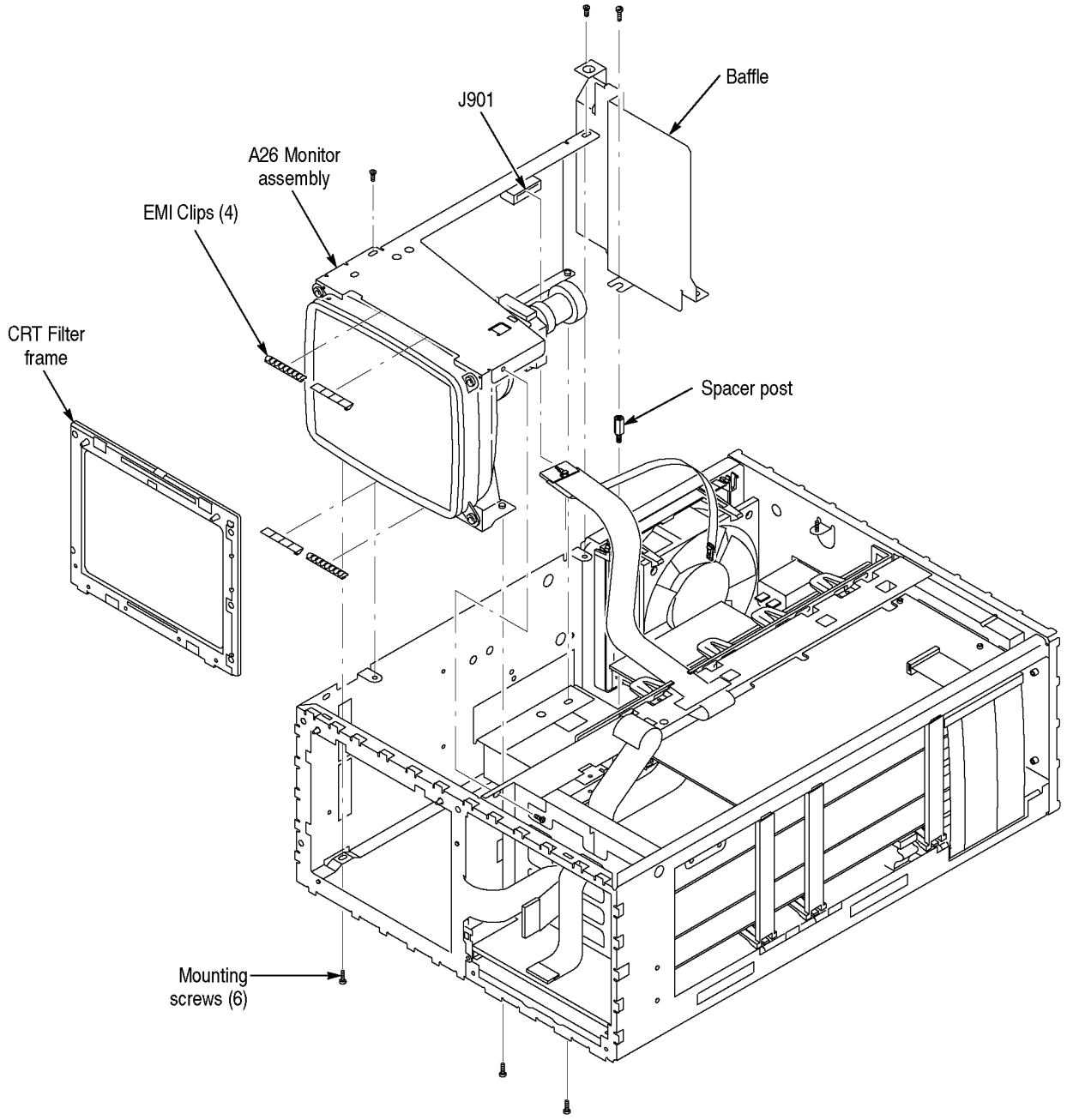


Figure 6-21: A26 Monitor Assembly Removal

4. To reinstall the filter frame and monitor, perform steps 3a-3g in reverse order. If the EMI clips on the monitor are replaced, be sure to center them in the notched area of the top and bottom of the chassis.

Com Bus, Board Supports, and PCAT Bus

For this procedure, no tools are required.

1. If you have not already performed the *Access Procedure* and removed the modules as instructed, do so now.
2. Set the CTS so its left side is down, with its front facing to the left of you.
3. Press the snap lock at the bottom end of the board support and tilt the support outwards to remove from the chassis (see Figure 6-22). Repeat for the second and third board supports.

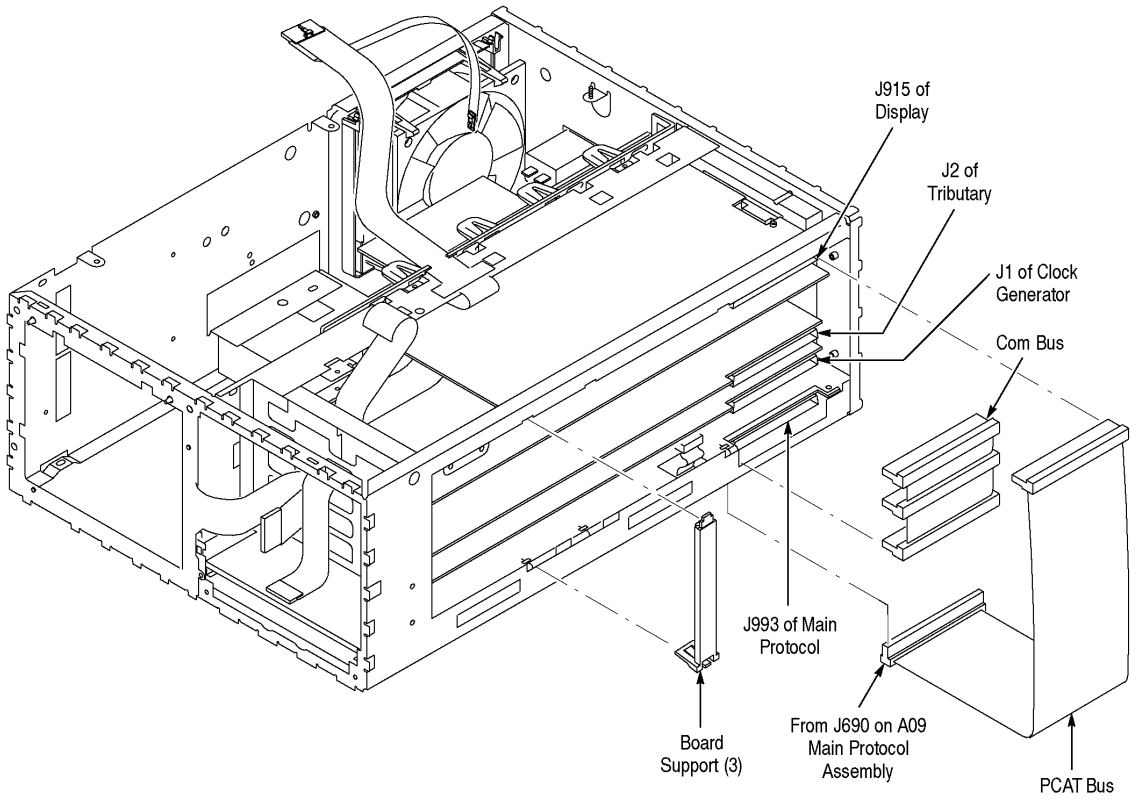


Figure 6-22: Com Bus, Board Supports, and PCAT Bus Removal

4. Grasp the PCAT bus by its cable pull tab and pull to unplug it from J915 of the Display assembly. Then grasp the connector and pull to unplug it from J690 of the A09 Lo-Speed Protocol assembly .

CAUTION: *Do not pull on the cable. Pulling on the cable will damage the cable or connector.*

5. Grasp the Com Bus connector, and pull to unplug it from J2 of the Tributary assembly and J1 of the A08 Clock Generator assembly. Then grasp the connector, and pull to unplug it from J993 of the A09 Lo-Speed Protocol assembly.

EMI Shield

For this procedure you will need a screwdriver with a size T–15 Torx tip and a flat–bladed screwdriver.

1. If you have not already performed the *Access Procedure* and removed the modules as instructed, do so now.
2. Set the CTS so its bottom is down, with its back facing you.
3. To remove the EMI shield, perform the following steps using Figure 6-23 as a guide:
    a. Working from the rear of the CTS, remove the five T–15 Torx–drive screws that secure the EMI Shield to the rear of the chassis.
    b. Insert the flat–bladed screwdriver in the corners of the shield near the center of the rear panel. Gently pry the edge of the shield away from the chassis.
    c. Working from the rear of the CTS, grasp the shield and pull it away from the CTS to complete its removal.
4. To reinstall the EMI shield, perform steps 3a-3c in reverse order. Make certain the edge of the EMI shield slides under the screws securing the board assemblies.

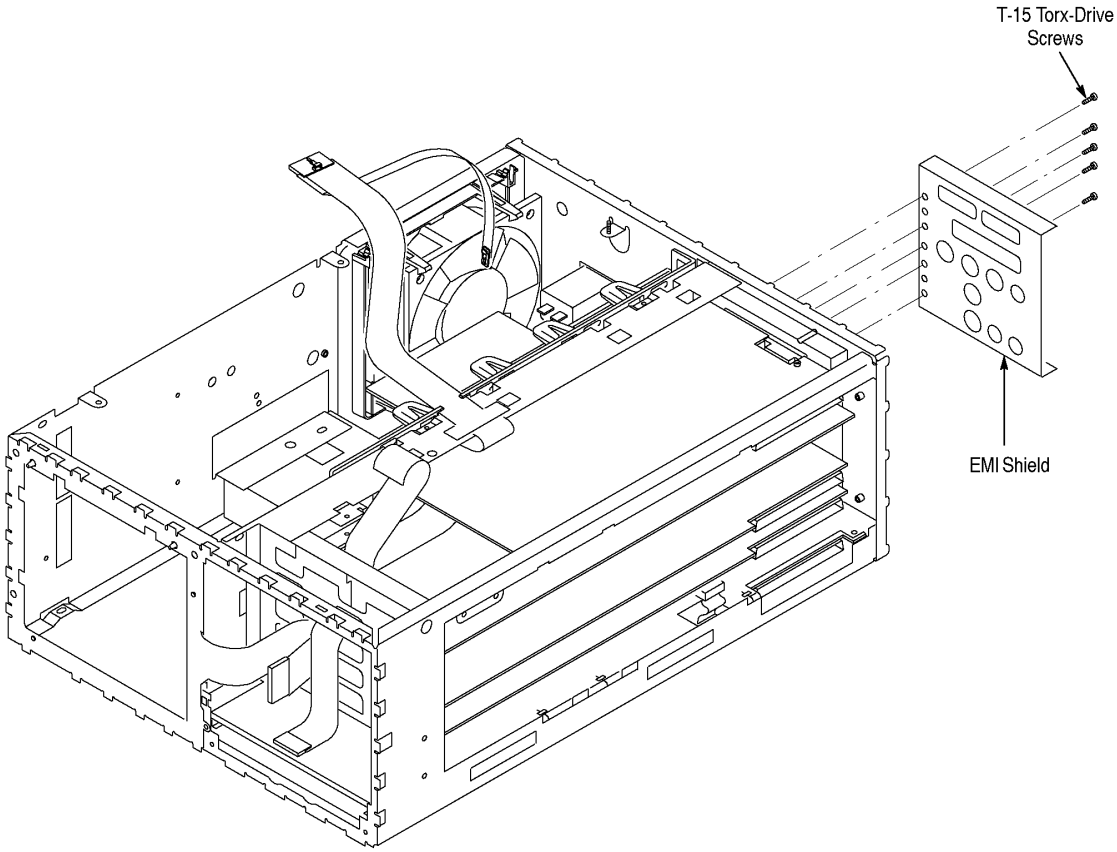


Figure 6-23: EMI Shield Removal

A01 Display/CPU Assembly

For this procedure you will need a screwdriver with a size T–15 Torx tip.

1. If you have not already performed the *Access Procedure* and removed the modules as instructed, do so now.
2. Set the CTS so its left side is down, with its front facing to the left of you.
3. To remove the A01 Display/CPU assembly, perform the following steps using Figure 6-24 as a guide:
    a. Unplug the monitor–to–display cable at J201.
    b. Lift up on the two locking tabs on J1 of the disk drive.
    c. Remove the cable from the disk drive.
    d. Remove the single T–15 Torx–drive screw from the bracket that secures the A01 Display/CPU assembly at the inside rear corner of the main chassis.
    e. Grasp the board by its edge, and pull outward to unplug it from J1 of the A02 Backplane assembly to complete the removal.

f. Lift up on the two locking tabs on J60 of the A01 Display assembly. Remove the cable from the A01 Display/CPU assembly.

4. To reinstall the A01 Display/CPU assembly, perform steps 3a-3f in reverse order.

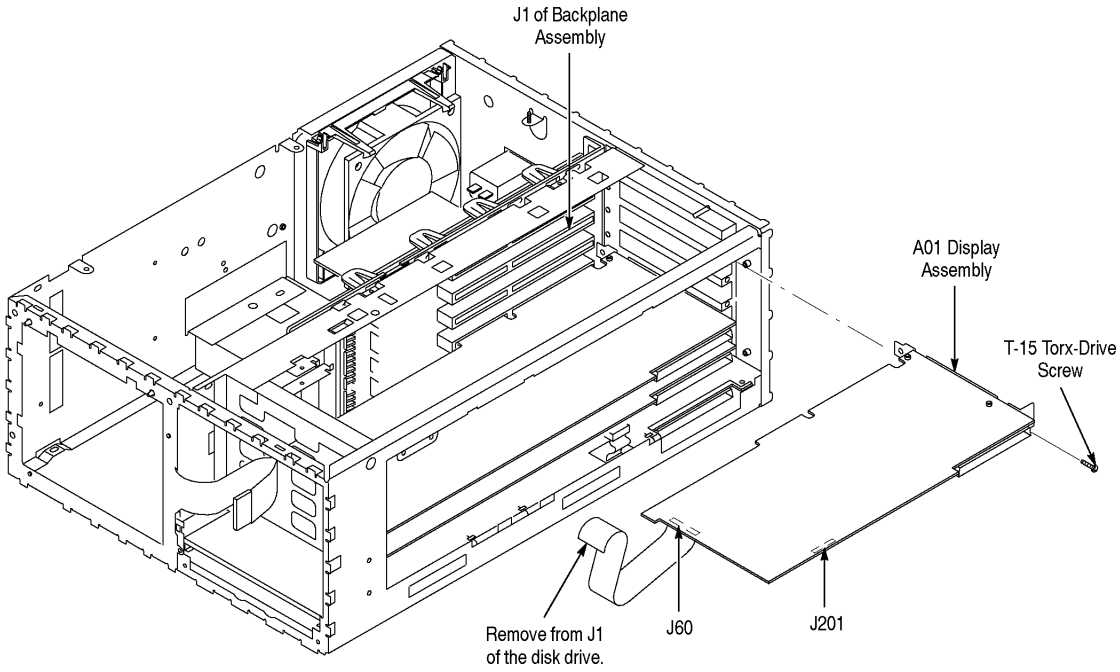


Figure 6-24: A01 Display/CPU Assembly Removal

A08 Clock Generator Assembly

For this procedure you will need a screwdriver with a size T–15 Torx tip.

1. If you have not already performed the *Access Procedure* and removed the modules as instructed, do so now.
2. Set the CTS so its left side is down, with its front facing to the left of you.
3. To remove the A08 Clock Generator assembly, perform the following steps using Figure 6-25 as a guide:
    a. Unplug the Main Protocol–to–Clock Generator cable at J2 of the A08 Clock Generator assembly.
    b. Remove the single T–15 Torx–drive screw from the bracket that secures the A08 Clock Generator assembly at the inside rear corner of the main chassis.
    c. Grasp the board by its edge, and pull upward to unplug it from J5 of the backplane assembly.

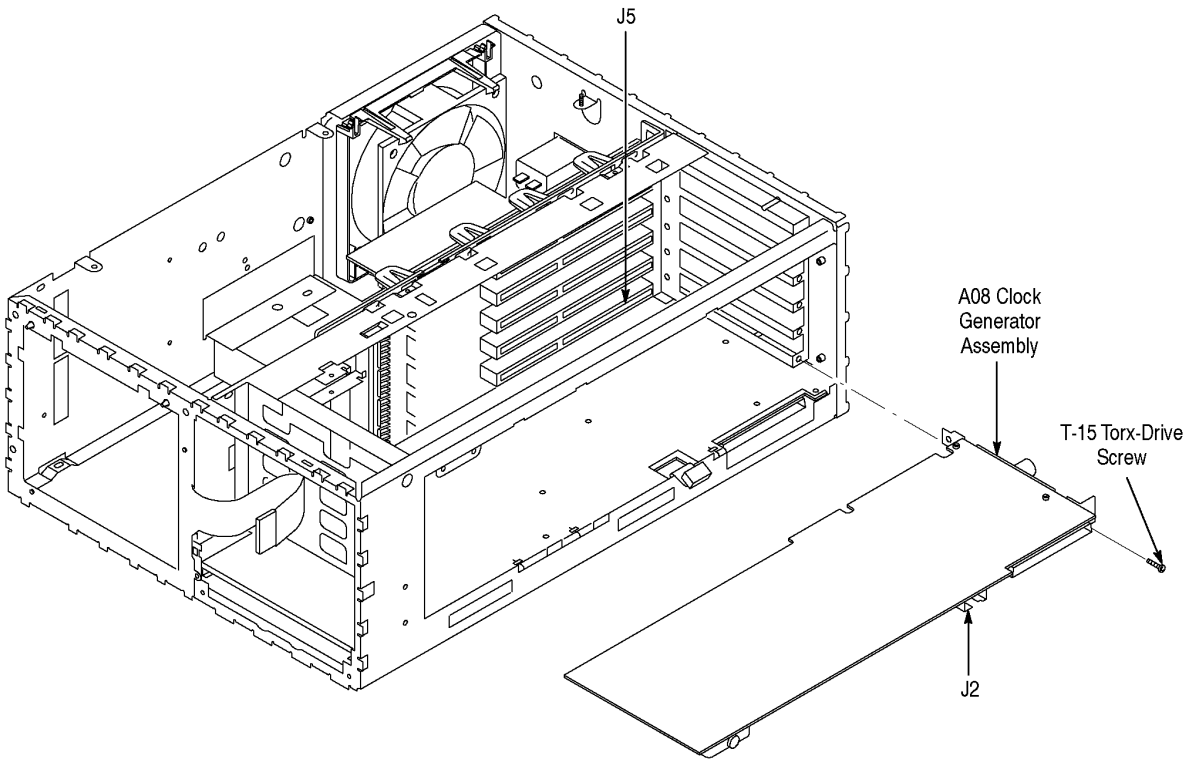


Figure 6-25: A08 Clock Generator Removal

d. As you remove the assembly, you will need to tilt it slightly so that the rear connectors can clear the chassis. Slide the assembly out of the chassis to complete the removal.

4. To reinstall the A08 Clock Generator assembly, perform steps 3a-3d in reverse order.

E1/E2/E3 Tributary and E4 Trib Assembly

For this procedure you will need a screwdriver with a size T–15 Torx tip.

1. If you have not already performed the *Access Procedure* and removed the modules as instructed, do so now.

2. Set the CTS so its left side is down, with its front facing to the left of you.

3. To remove the E1/E2/E3 and E4 Tributary assemblies, perform the following steps using Figure 6-26 as a guide:

a. Unplug the Tributary–to–front– and rear–panel cables from the Tributary assembly (J225, J217, J218, and J220 on Option 22; J225, J5, J6, and J7 on Option 36).

b. Remove the single T–15 Torx–drive screw from the bracket covering the center rear–panel slot at the inside rear corner of the main chassis.

c. Remove the single T–15 Torx–drive screw from the bracket that secures the Tributary assembly at the inside rear corner of the main chassis.

d. Grasp the board by its edges, and pull upward to unplug it from the backplane assembly.

e. Slide the board the rest of the way out of the main chassis to complete its removal.

4. To separate the E1/E2/E3 and the E4 Tributary PCBs, perform the following steps:

a. Remove the five T-15 Torx-drive screws from the E4 PCB.

b. Mark each MMS connector with the appropriate location and gently remove each cable.

c. Carefully pry apart the three 100-pin connectors to separate the PCBs.

5. To reinstall the E1/E2/E3 Tributary assembly, perform steps 3a-3e in reverse order. To reconnect the E1/E2/E3 and E4 PCBs, perform steps 4a-4c in reverse order.

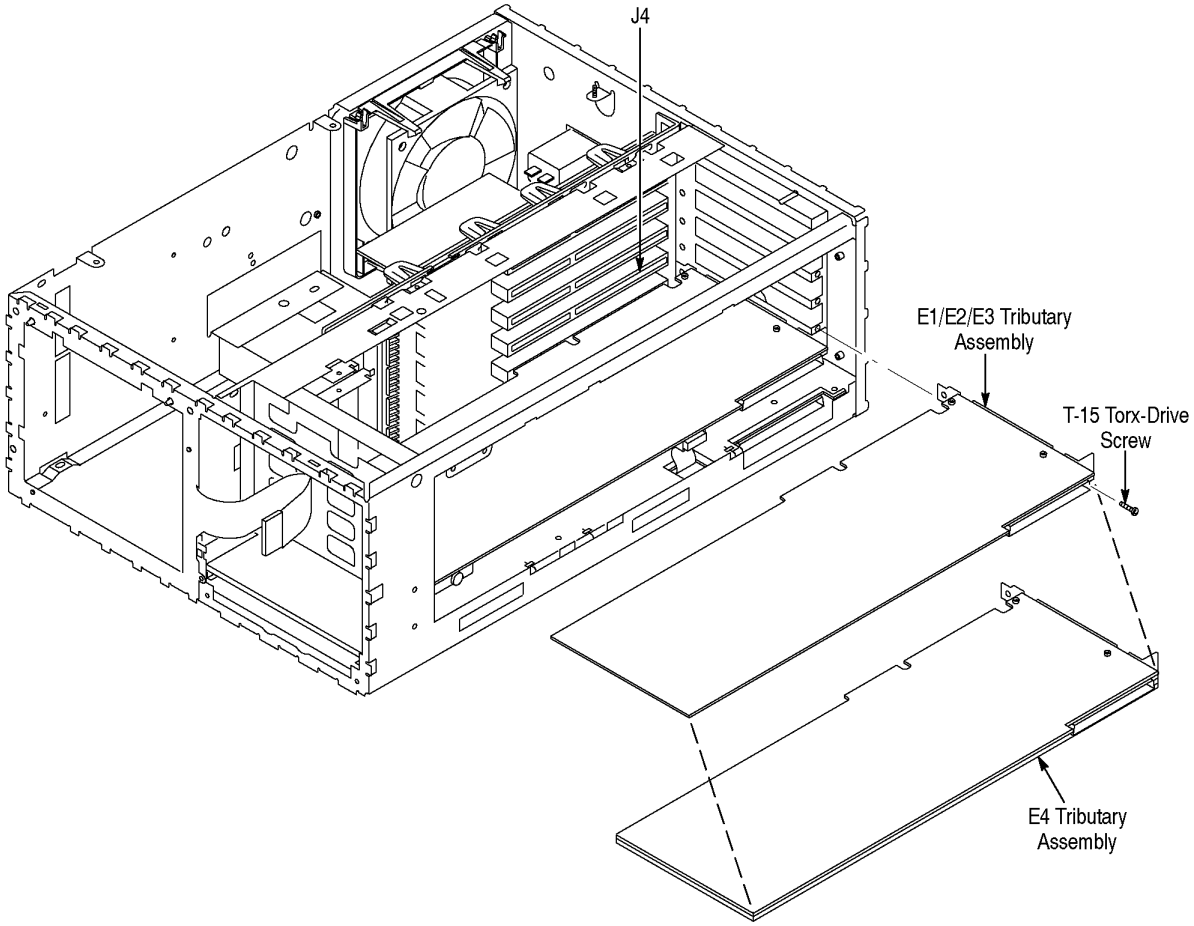


Figure 6-26: E1/E2/E3 Tributary and E4 Trib Removal

JAWA/JAWG Assembly

For this procedure you will need a screwdriver with a size T–15 Torx tip.

1. If you have not already performed the *Access Procedure* and removed the modules as instructed, do so now.
2. Set the CTS so its left side is down, with its front facing to the left of you.
3. To remove the JAWA/JAWG assembly, perform the following steps using Figure 6-27 as a guide:
    a. Unplug the cables to the JAWA/JAWG assembly (J130, J140, J142, J150, J230, J240, J260, and J270).
    b. Remove the single T–15 Torx–drive screw from the bracket covering the center rear–panel slot at the inside rear corner of the main chassis.

c. Remove the single T–15 Torx–drive screw from the bracket that secures the JAWA/JAWG assembly at the inside rear corner of the main chassis.

d. Grasp the board by its edges, and pull upward to unplug it from the backplane assembly.

e. Slide the board the rest of the way out of the main chassis to complete its removal.

4. To reinstall the JAWA/JAWG assembly, perform steps 3a-3e in reverse order. To reconnect the JAWA/JAWG PCBs, perform steps 4a-4c in reverse.

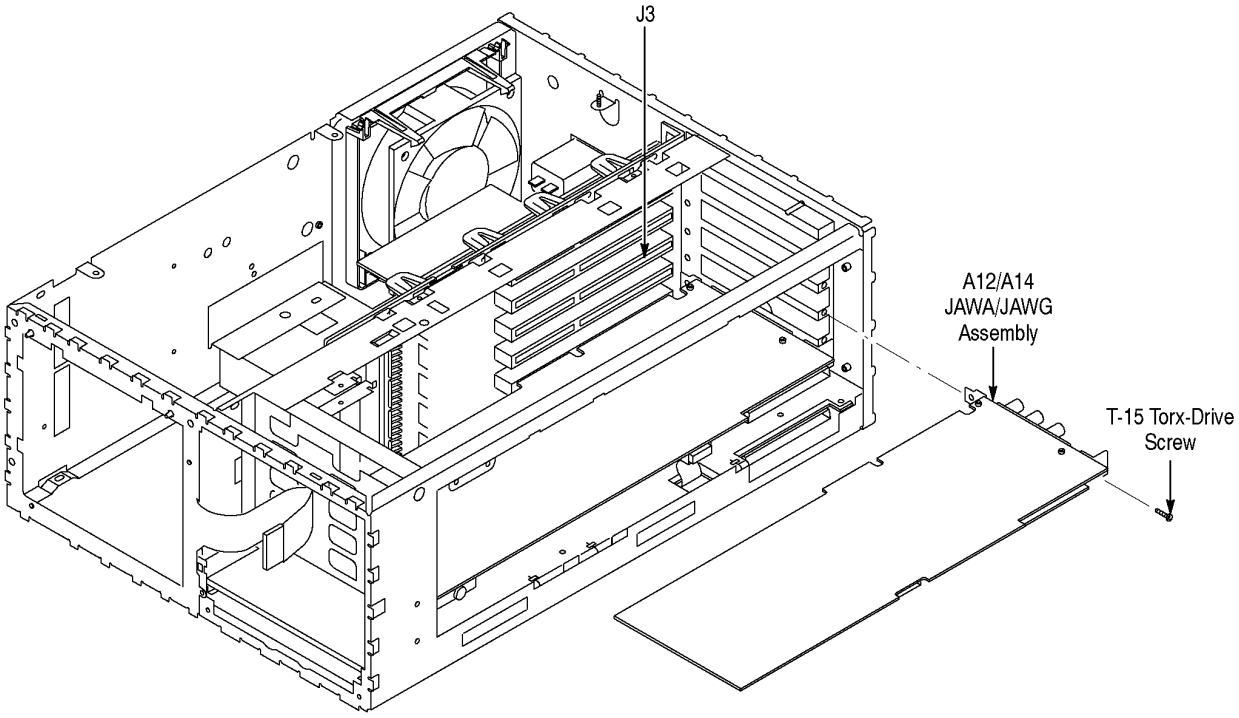


Figure 6-27: JAWA/JAWG Removal

A02 Backplane Assembly

For this procedure you will need a screwdriver with a size T–15 Torx tip and a flat–bladed screwdriver.

1. If you have not already performed the *Access Procedure* and removed the modules as instructed, do so now.
2. Set the CTS so its left side is down, with its front facing to the left.
3. To remove the A02 Backplane assembly, perform the following steps using Figure 6-28 as a guide:
    - **a.** Remove any unused board brackets, mounted on the rear panel, that correspond to unused board slots in the Backplane assembly. To remove the bracket, remove the single T–15 Torx–drive screw that secures the bracket at the inside rear corner of the main chassis.
    - **b.** Unplug the Backplane–to–Low Voltage Power Supply–to–Main Protocol cable at J7 of the A02 Backplane assembly.
    - **c.** Unplug the Backplane–to–AUX power cable at J6 of the A02 Backplane assembly.
    - **d.** Remove the five T15 Torx–drive screws mounting the board to the chassis.
    - **e.** Turn the CTS so its bottom is facing down on the work surface. Leave its front facing to the left.
    - **f.** Find the flex lock nearest the front of the CTS (shown in Figure 6-7). Using a flat–bladed screwdriver, push the flex lock so it flexes enough to clear the board.
    - **g.** While holding the flex lock, slightly pull up on the front corner of the board nearest that retainer until it clears that flex lock. Repeat for the remaining three flex locks.
    - **h.** Once the board is clear of all four flex locks, grasp the board by the edge near those flex locks, rotate that edge upwards slightly, and pull the board out of its retainer slot at its opposite edge.
    - **i.** Lift the assembly all of the way out of the chassis to complete the removal.
4. To reinstall the A02 Backplane assembly, perform steps 3a-3i in reverse order. Be sure to align the board to the retainer slot when doing step 3h. Seat the board until the four retainers snap over the edge of the Backplane assembly when doing step 3g.

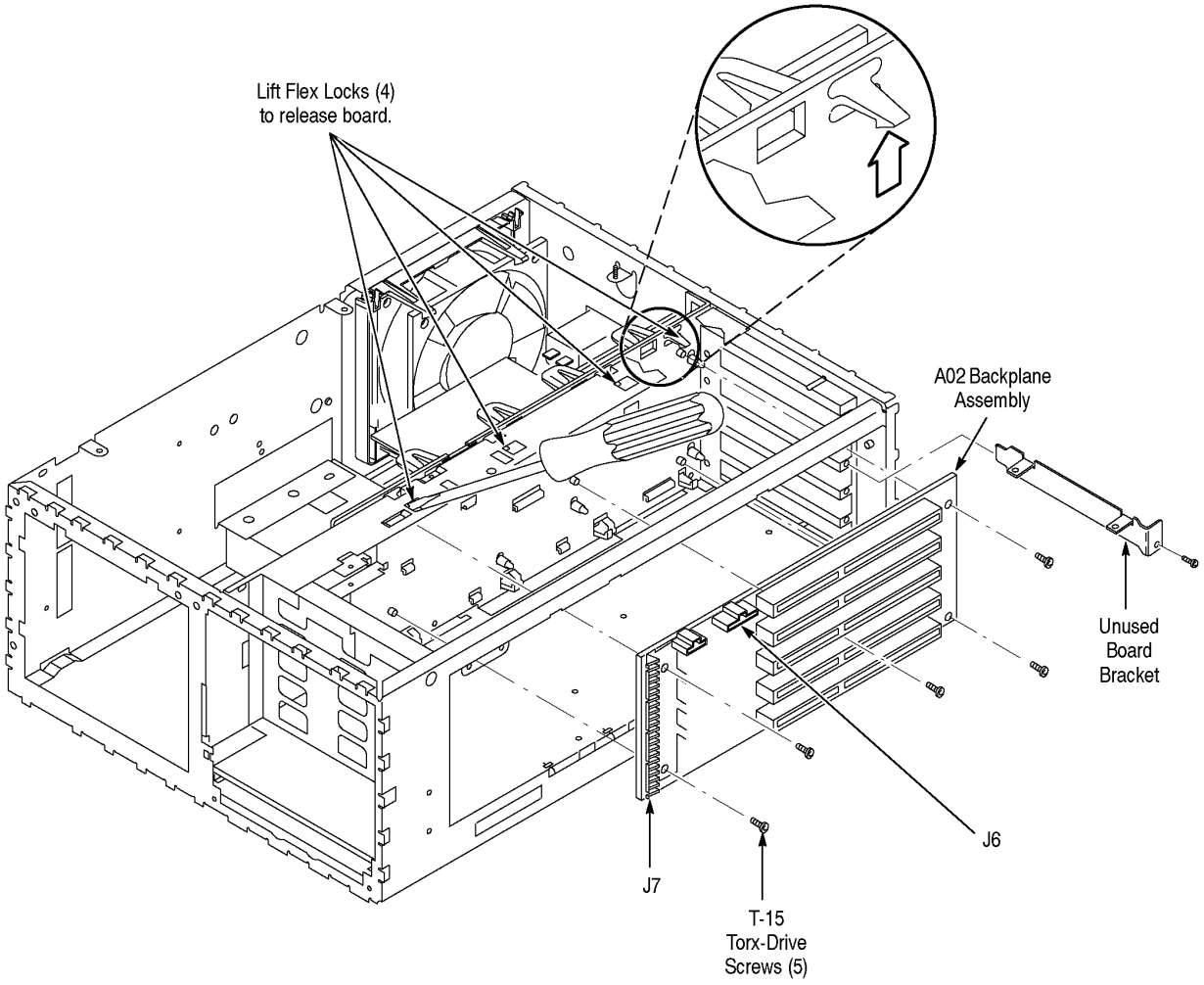


Figure 6-28: A02 Backplane Assembly

Back-up Battery

When you disconnect the battery, you will lose all saved front panel setups. Adjustment constants, stored internally when the CTS is adjusted, are not lost.

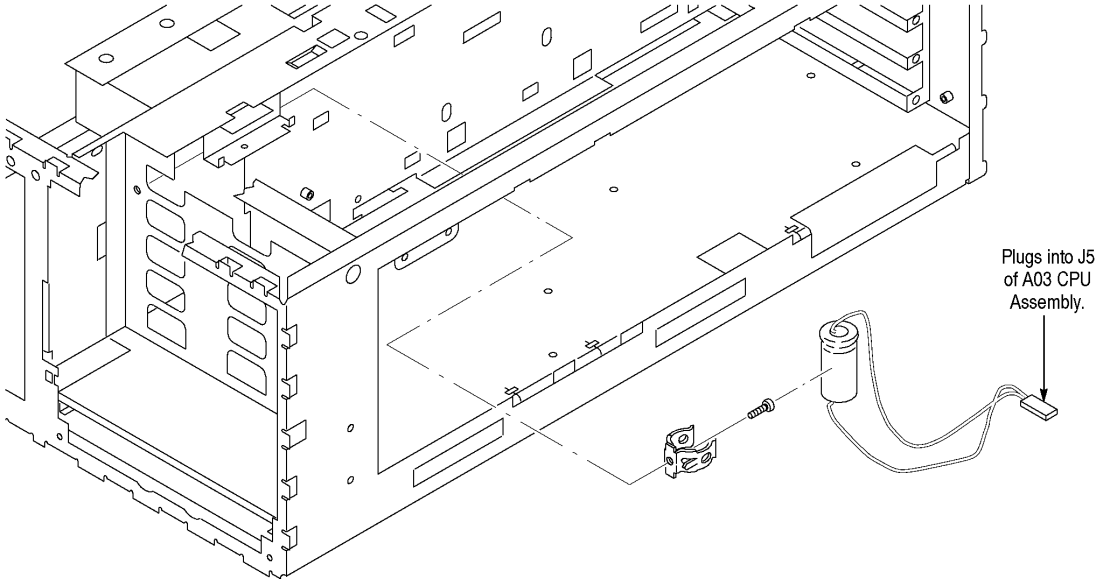
For this procedure you will need a screwdriver with a size T–15 Torx tip.

CAUTION: *The battery used in this CTS can present a fire or chemical burn hazard if mistreated. Do not recharge, rapidly discharge, disassemble, heat above 100° C, or incinerate. Replace the battery with the part number listed in the Mechanical Parts List section only. Use of another battery may present a risk of fire or explosion.*

Dispose of used batteries promptly. Small quantities of used batteries may be disposed of in normal refuse. Keep away from children. Do not disassemble and do not dispose of in fire.

1. If you have not already performed the *Access Procedure* and removed the modules as instructed, do so now.
2. Set the CTS so its top is down on the work surface, with its right side facing you.
3. To remove the back–up battery, pull the battery out of its clamp near the front of the chassis, see Figure 6-29.
4. If removing the battery retainer, remove the T–15 Torx–drive screw from the battery retainer. Lift the battery retainer out of the chassis to complete its removal.

Figure 6-29: Battery Removal



5. To reinstall the battery and its retainer, perform steps 2 and 3 in reverse order.

Fan and Fan Mount

For this procedure, no tools are required.

1. If you have not already performed the *Access Procedure* and removed the modules as instructed, do so now.
2. Set the CTS so its bottom is down, with its rear facing you.
3. To remove the fan, perform the following steps using Figure 6-30 as a guide:
    a. Unplug the fan power cable from J3 on the Auxiliary Power Supply.
    b. Release the two flex locks securing the top of the fan to the fan mount (shown in Figure 6-30); then lift the fan out from the top of the chassis.

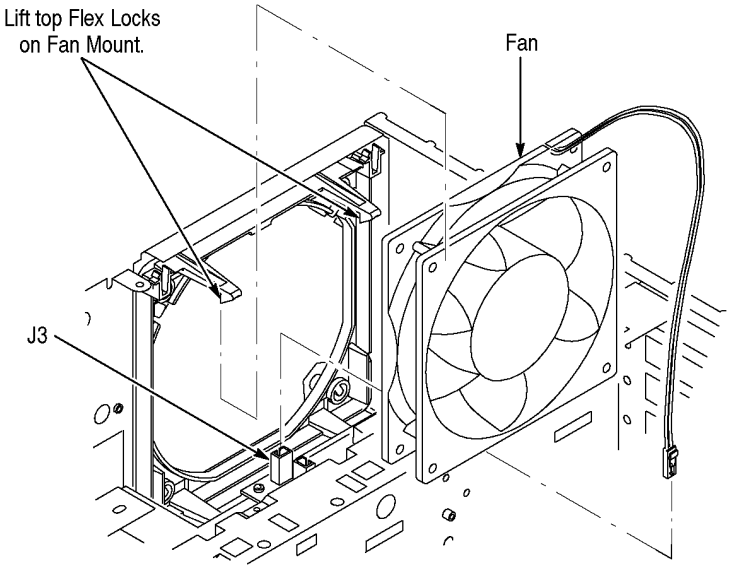


Figure 6-30: Fan Removal

NOTE: *Do not do step 4 unless servicing a broken fan mount or removing the mount for cleaning.*

4. To remove the fan mount, perform the following steps using Figure 6-10 as a guide:
    a. Rotate the CTS so the side that houses the fan mount is facing upwards.
    b. Press the two flex locks to release them (see Figure 6-31).

c. While holding the flex locks released, slide the fan mount so its four retainer lugs slide from their small retainer holes in the chassis into their large release holes.

d. Move the fan mount inward so its retainer lugs are out of the large retainer holes, and lift it out of the chassis to remove.

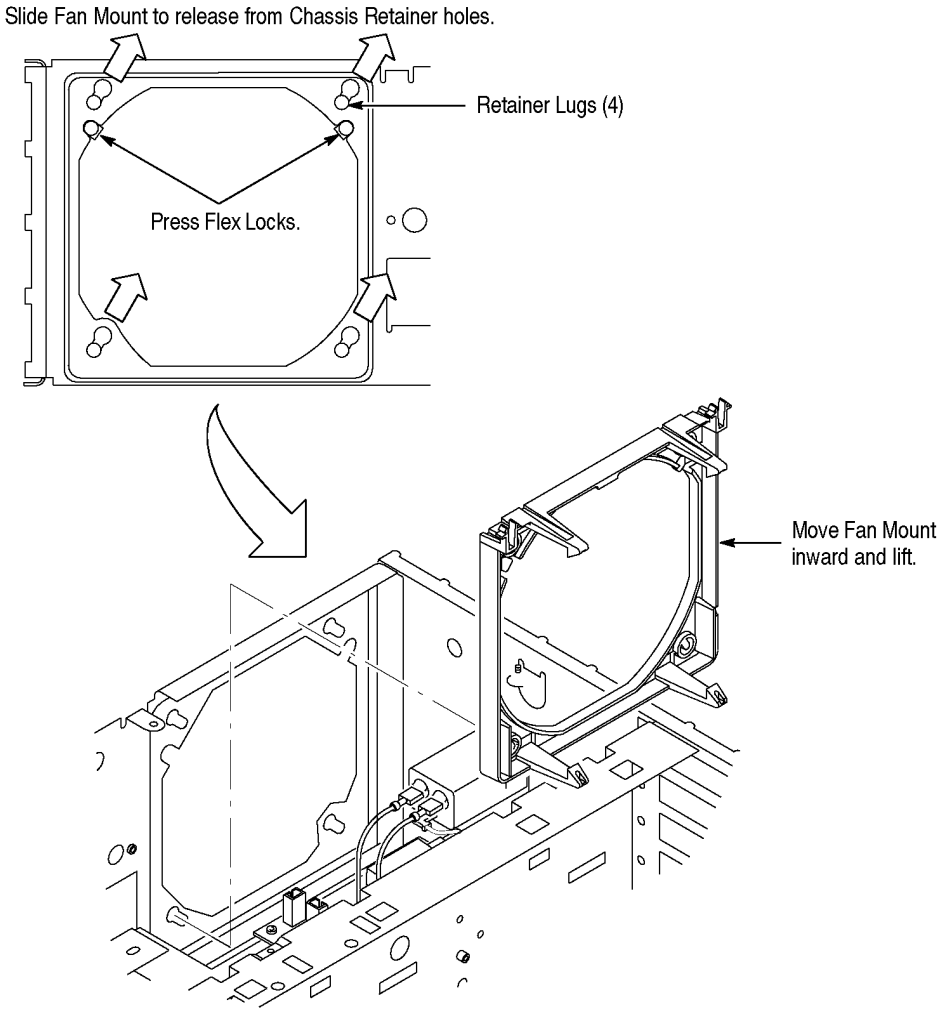


Figure 6-31: Fan Mount Removal

5. To reinstall the fan and its mount, perform the following steps:

a. If the fan mount was removed, perform steps 4a-4d in reverse order. Be sure to seat the fan mount so its two flex locks snap to secure it on the chassis.

b. To reinstall the fan, perform steps 3a-3b in reverse order. Be sure the two locks snap into place to secure the fan.

A25 Low Voltage Power Supply and its Mount

For this procedure you will need a screwdriver with a size T–15 Torx tip and a pair of duck–bill pliers.

1. If you have not already performed the *Access Procedure* and removed the modules as instructed, do so now.
2. Set the CTS so its bottom is down on the work surface, with its front facing to the right.

CAUTION: *When releasing the Low Voltage Power Supply from its mount, take care not to push on the board components. Rather, push on the board edge when performing the following steps.*

3. To remove the Low Voltage Power Supply, perform the following steps using Figure 6-32 as a guide:
    - **a.** Unplug the cable coming from the Backplane assembly at J2.
    - **b.** Unplug the cable coming from the AUX power supply at J1.
    - **c.** Unplug the AUX power cable at J7 on the A07 Auxiliary Power supply.
    - **d.** Unplug the monitor cable at J4 on the A07 Auxiliary Power supply.
    - **e.** Now, release and disconnect the remote–power cable where it joins the cable from the Low Voltage Power Supply assembly.
    - **f.** Working through the opening created when the fan was removed, remove the T–15 Torx–drive screw at the center of the power supply board.
    - **g.** Using a pair of duck–bill pliers, squeeze to release each of the four flex locks at the top edge of the Low Voltage Power Supply assembly.
    - **h.** Once released, tilt the board out away from the flex locks, and then unplug the AC power cable (remote power switch) where it connects to the cable from the Low Voltage Power Supply (J4).
    - **i.** Lift the Low Voltage Power Supply assembly out of the chassis to complete its removal.

NOTE: *Do not do step 4 unless servicing a broken power supply mount or removing the mount for cleaning.*

4. To remove the power–supply mount, perform the following steps:

a. Place the CTS so its left side is down, with its top facing you.

b. Press the two retainer locks, and slide the power–supply mount towards the top of the CTS to unlock from the chassis.

c. Lift the power–supply mount out of the chassis to complete the removal.

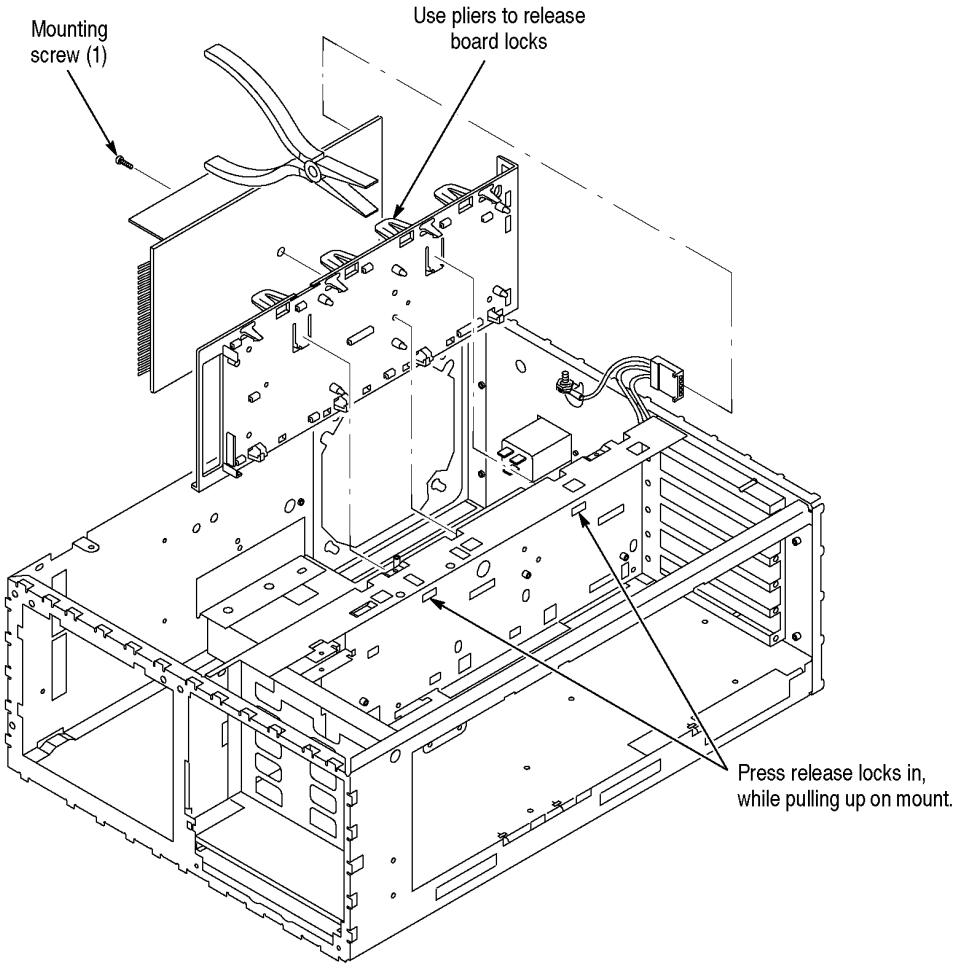


Figure 6-32: A25 Low Voltage Power Supply Removal

5. To reinstall the Low Voltage Power Supply and its mount, perform the following steps:

    a. If the power supply mount was removed, perform steps 4a-4c in reverse order. When reinstalling the power–supply mount, be sure to press it flush against the chassis before sliding it towards the bottom of the chassis to lock.

    b. To reinstall the Low Voltage Power Supply, perform steps 3a-3i in reverse order. Be sure to seat the board until all four flex locks are locked.

Line Filter

For this procedure you will need a screwdriver with a size T–15 Torx tip.

1. If you have not already performed the *Access Procedure* and removed the modules as instructed, do so now.
2. Set the CTS so its bottom is down on the work surface, with its rear facing you.
3. To remove the line filter, perform the following steps using Figure 6-33 as a guide:

    a. Unplug the three connectors at the line filter.

    b. Remove the two screws mounting the line filter to the chassis. Pull the filter out through the rear of the chassis to complete the removal.

WARNING: *When reconnecting the Auxiliary Power Supply to the line filter, be sure to connect the neutral side of the line filter to the white–striped lead and the load side to the black–striped lead.*

It is not necessary to disconnect the earth ground from the chassis lug that it is bolted to. If, however, you have done so, be sure to install the earth lead (and its nut) from the line filter before installing the earth lead (and its nut) from the Low Voltage Power Supply.

4. To reinstall the line filter, perform steps 3a-3b in reverse order. When finished, reverify that the wires from the Auxiliary Power Supply assembly are connected correctly.

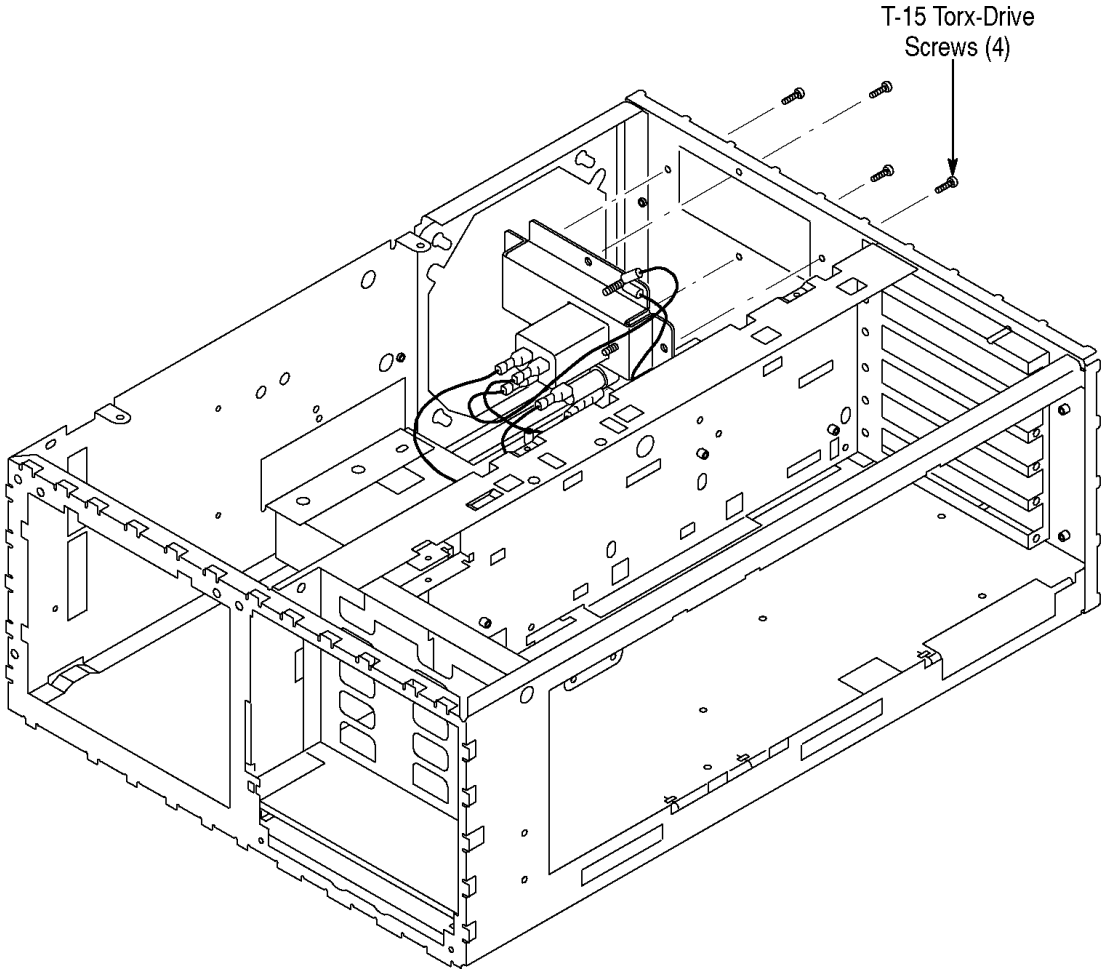


Figure 6-33: Line Filter Removal

Main Chassis

Since the removal of the main chassis requires the removal of virtually all modules, perform the procedure *Disassembly for Cleaning* that follows. To reinstall the main chassis, see reinstallation instructions in *Disassembly for Cleaning*.

Disassembly for Cleaning

This procedure is for disassembly of the CTS 800–Series Test Set into its individual modules so they can be cleaned. Read the cleaning instructions in *Inspection and Cleaning* of this section before disassembling the CTS.

For this procedure you will need a screwdriver with a T–15 Torx tip, a T–20 Torx tip , a flat–bladed screwdriver , a hex key screwdriver , duck–bill pliers , spudger , a Pozidriv screwdriver , and a soldering iron .

1. Familiarize yourself with the modules illustrated in Figures 6-3, 6-4, & 6-5.
2. To completely disassemble the CTS, perform the following procedures in the order listed. They are found under *Procedures for Module Removal and Installation* which start.
    - **a.** *Line Fuse*
    - **b.** *Front Cover, Rear Cover, Cabinet, Rear EMI Gasket, and Cabinet Handle and Feet*
    - **c.** *Plug–In Interface Module*
    - **d.** *Disk Drive*
    - **e.** *Trim Ring, Menu Elastomer, Menu Buttons, and Front EMI Gaskets*
    - **f.** *A06 Front Panel Assembly and Menu Flex Circuit*
    - **g.** *Fan and Fan Mount*
    - **h.** *A25 Low Voltage Power Supply and its Mount*
    - **i.** *A26 Monitor Assembly*
    - **j.** *Line Filter*
    - **k.** *EMI Shield*
    - **l.** *Com Bus, Board Supports, and PCAT Bus*
    - **m.** *A08 Clock Generator Assembly*
    - **n.** E1/E2/E3 *Tributary and E4 Trib Assembly*
    - **o.** *A12/A14 JAWA/JAWG Assembly*
    - **p.** *A01 Display/CPU Assembly*
    - **q.** *A02 Backplane Assembly*

r. *Back–Up Battery*

s. *A10 Hi-Speed Protocol Assembly*

t. *A09 Lo-Speed Protocol Assembly*

3. To completely reassemble the CTS, perform the following procedures in the order listed. Observe these general instructions as you perform them:

- When doing the listed procedures, perform their steps in reverse order.
- When reinstalling the modules, ignore any instructions that require connecting a cable or bus to a module that you have not yet installed. You will make the necessary connections when you install the missing module.
- Ignore any instructions to do the *Access Procedure*. The access procedure is only used when removing individual modules for servicing, not when doing a disassembly/reassembly for cleaning.

a. *A09 Lo-Speed Protocol Assembly*

b. *A10 Hi-Speed Protocol Assembly*

c. *Line Filter*

d. *A26 Monitor Assembly*

e. *A25 Low Voltage Power Supply and its Mount*

f. *Fan and Fan Mount*

g. *Back–Up Battery*

h. *A02 Backplane Assembly*

i. *A01 Display/CPU Assembly*

j. *A12/A14 JAWA/JAWG Assembly*

k. E1/E2/E3 *Tributary and E4 Trib Assembly*

l. *A08 Clock Generator Assembly*

m. *EMI Shield*

n. *Com Bus, Board Supports, and PCAT Bus*

o. *A06 Front Panel Assembly and Menu Flex Circuit*

p. *Trim Ring, Menu Elastomer, Menu Buttons, and Front EMI Gaskets*

q. *Disk Drive*

r. *Front Cover, Rear Cover, Cabinet, Rear EMI Gasket, and Cabinet Handle and Feet*

s. *Line Fuse*

Troubleshooting

This section contains information and procedures designed to help you isolate faulty modules in CTS850 Test Set. If a module needs to be replaced, follow the Removal and Replacement procedures in the previous section.

WARNING: *The CTS operates over several ranges of line voltage (see Power Requirements in the section on Specifications). Before stepping the line voltage from one range to a higher range, set the principal power switch (rear panel) to its* ***OFF*** *position. Failure to do so can damage the CTS.*

Diagnostics

The CTS self–test diagnostics help you verify, adjust, and, if necessary, isolate faulty modules. The error reporting tells you which module is bad or leads you, with the help of the troubleshooting procedures, to the bad module.

The CTS has two levels of internal diagnostics, power–up and extended. At power–up the CTS automatically executes the power–up diagnostics and reports any bad modules or interfaces. The extended set is user selectable and tests CTS circuitry in–depth. It also reports any bad modules or interfaces.

Table 6-7 lists the modules tested by the diagnostics.

Table 6-7: Modules Tested by Power–Up and Extended Diagnostics

Module
A01 Display
A02 Backplane
A03 CPU
Plug–In Interface Module
A06 Front Panel
A07 Auxiliary Power
A08 Clock Generator
A09 Main Protocol
A10 High Speed Protocol
A25 Low Voltage Power Supply
A11/A13 Tributary
A12/A14 JAWA/JAWG

Running Self Test

This procedure uses internal routines to verify that the CTS passes its internal self tests.

Equipment Required	No test equipment or connections are required
Prerequisites	Power up the CTS and allow a twenty minute warm–up period before running Self Test
Time Required	Approximately two minutes (after warm–up time)

Set up and execute the Self Test with the following sequence:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
UTILITY	SELF TEST	Self Test Group	Sys: Internal
		Self Test Control	Run

Troubleshooting Trees

Use this section in conjunction with the self test diagnostics to isolate a faulty module.

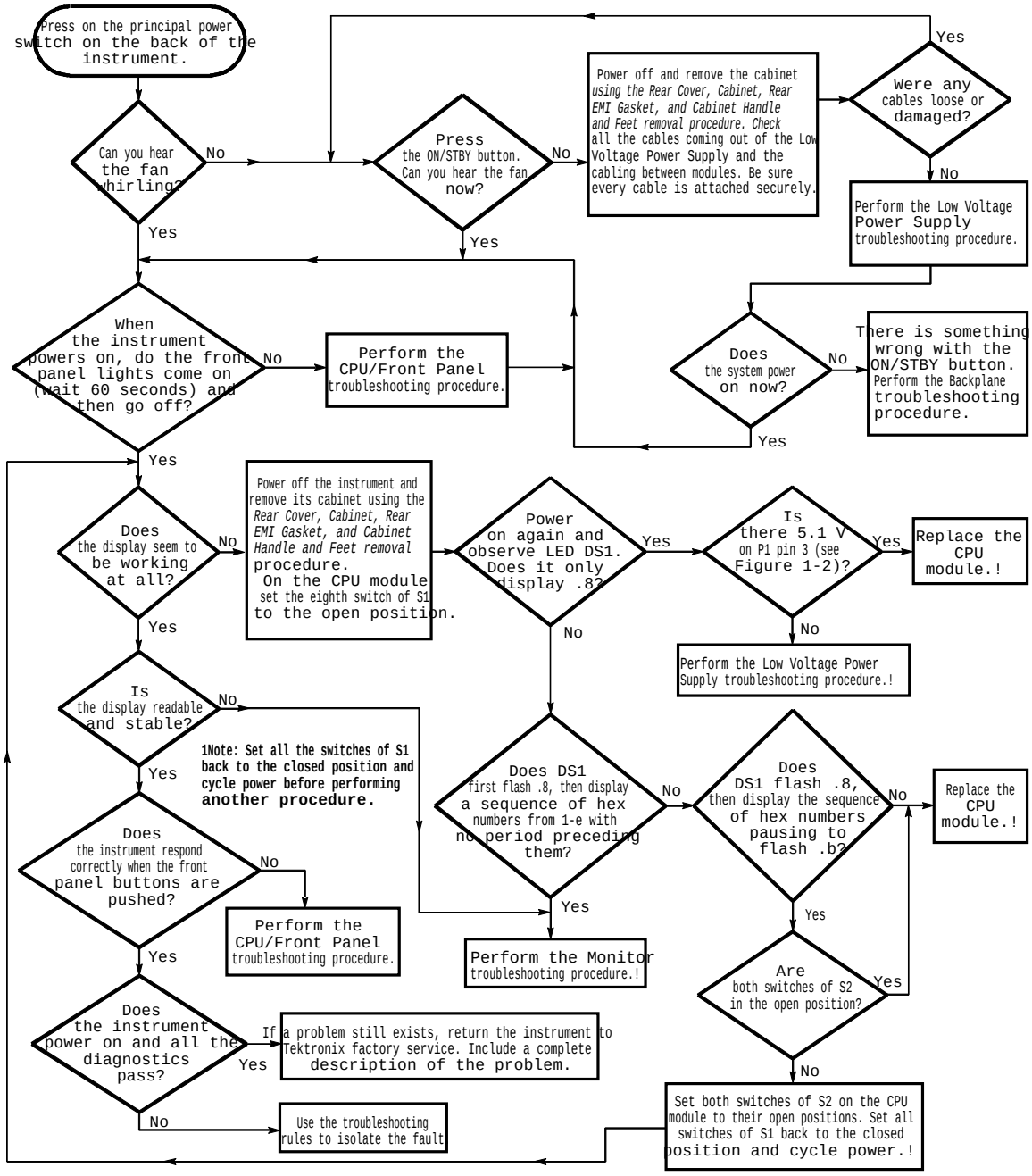


Figure 6-34: Primary Troubleshooting Procedure

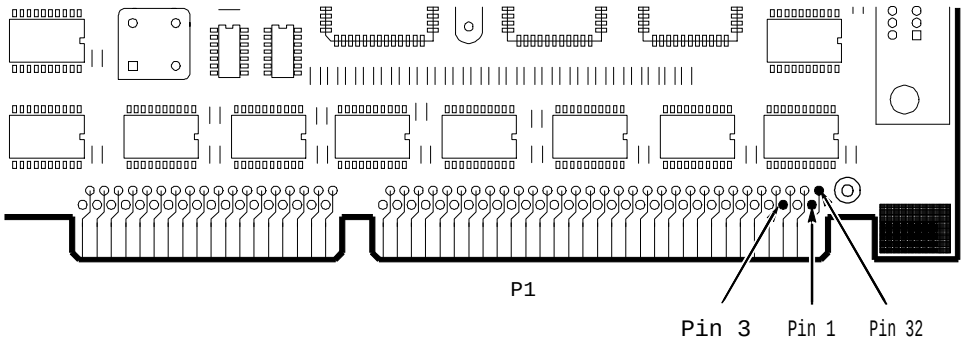


Figure 6-35: CPU Board Connector P1

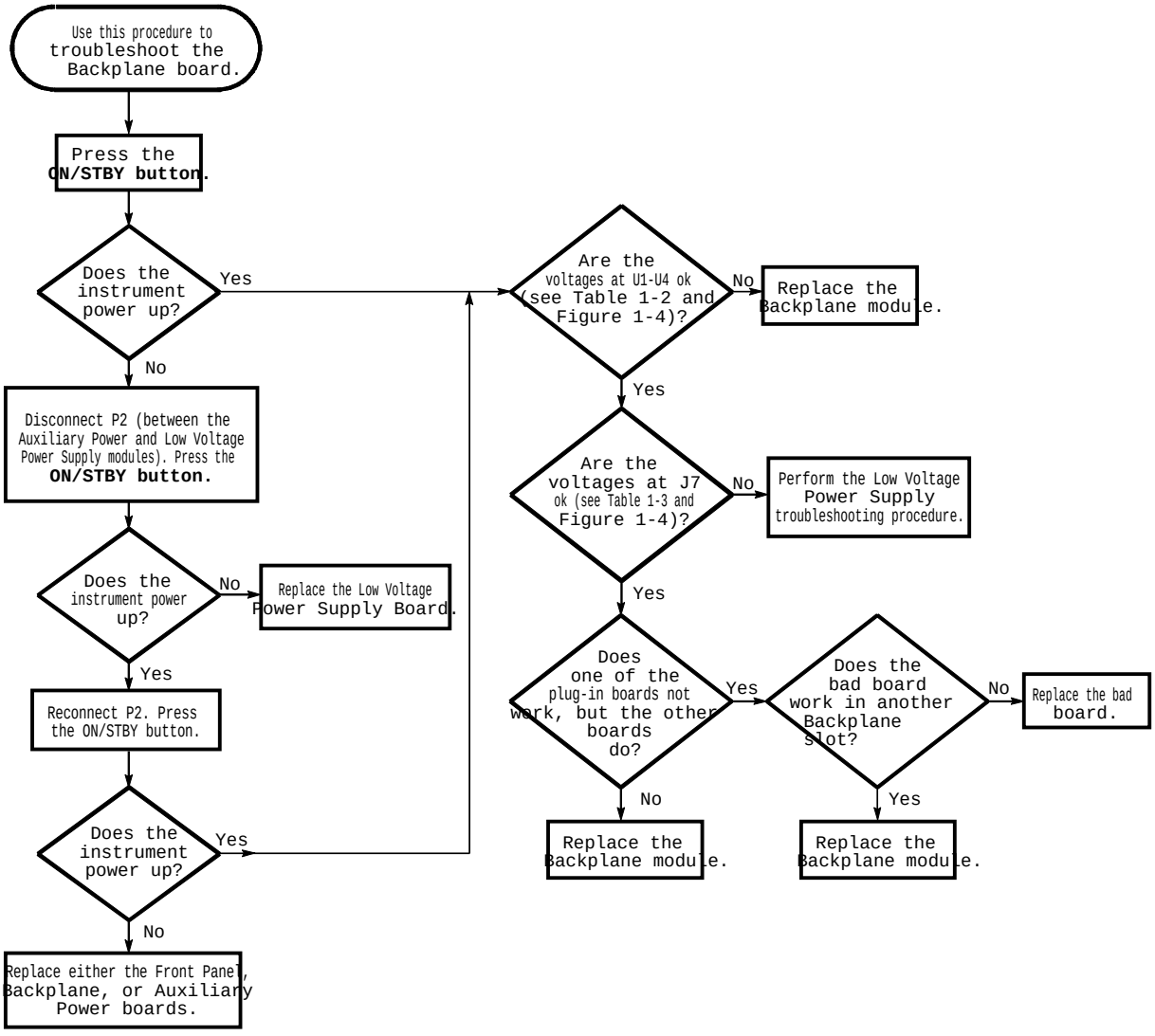


Figure 6-36: Backplane Troubleshooting Procedure

Table 6-8: Regulator Voltages

Regulator	Nominal Voltage	Minimum Voltage	Maximum Voltage
U1 pin 3	-12 V	-11.5 V	-12.5 V
U2 pin 3	+12 V	+11.5 V	+12.5 V
U4 pin 3	-6.4 V	-6.336 V	-6.464 V

Table 6-9: J7 Voltages

Pin	Nominal Voltage	Minimum Voltage	Maximum Voltage
1	-15 V	-14.85 V	-15.15 V
2	-15 V	-14.85 V	-15.15 V
7	-6.4 V	-6.336 V	-6.464 V
8	+15 V	+14.85 V	+15.15 V
9	+15 V	+14.85 V	+15.15 V
18	+5.1 V	+5.151 V	+5.05 V
19	+5.1 V	+5.151 V	+5.05 V

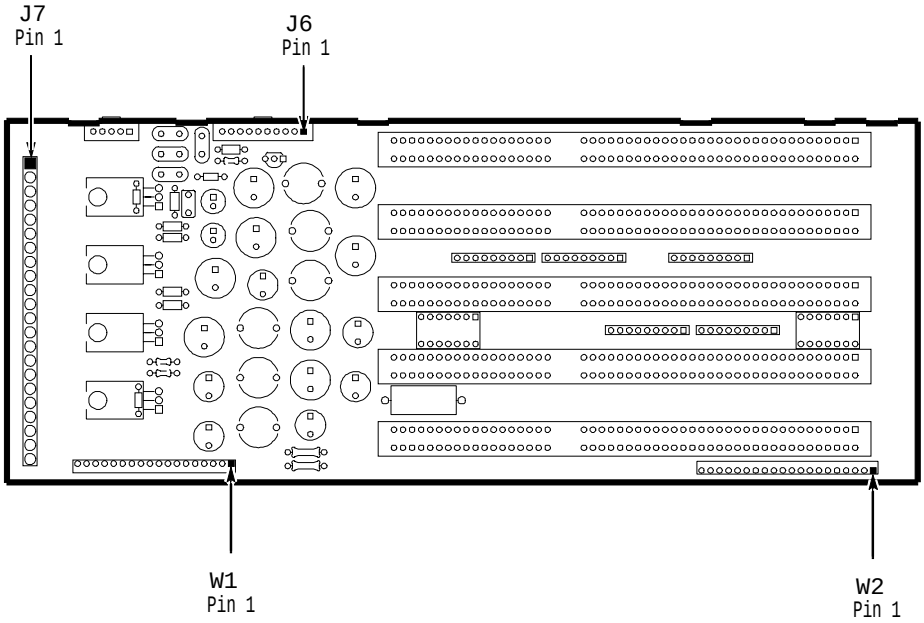


Figure 6-37: Backplane Module

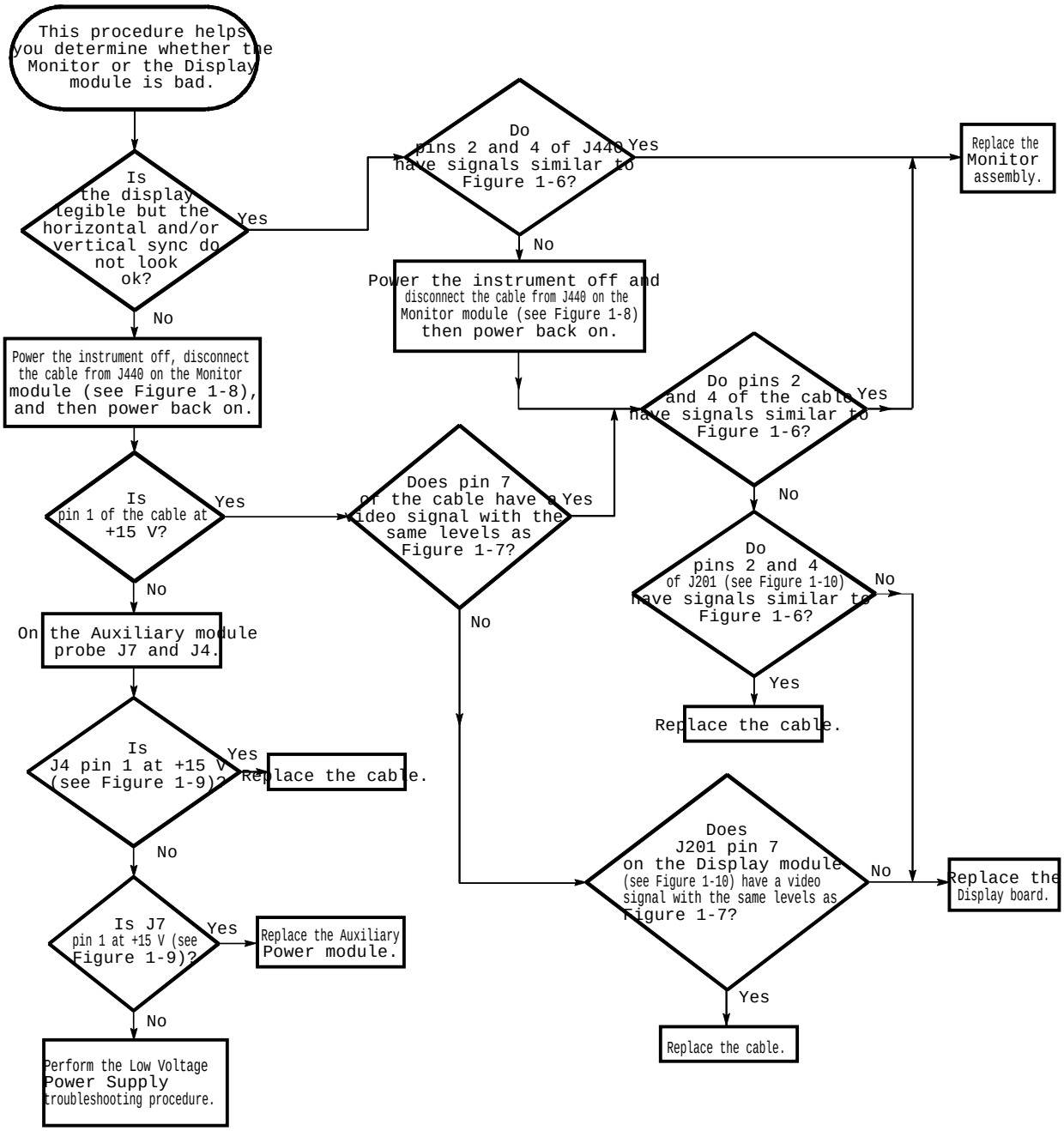


Figure 6-38: Monitor Troubleshooting Procedure

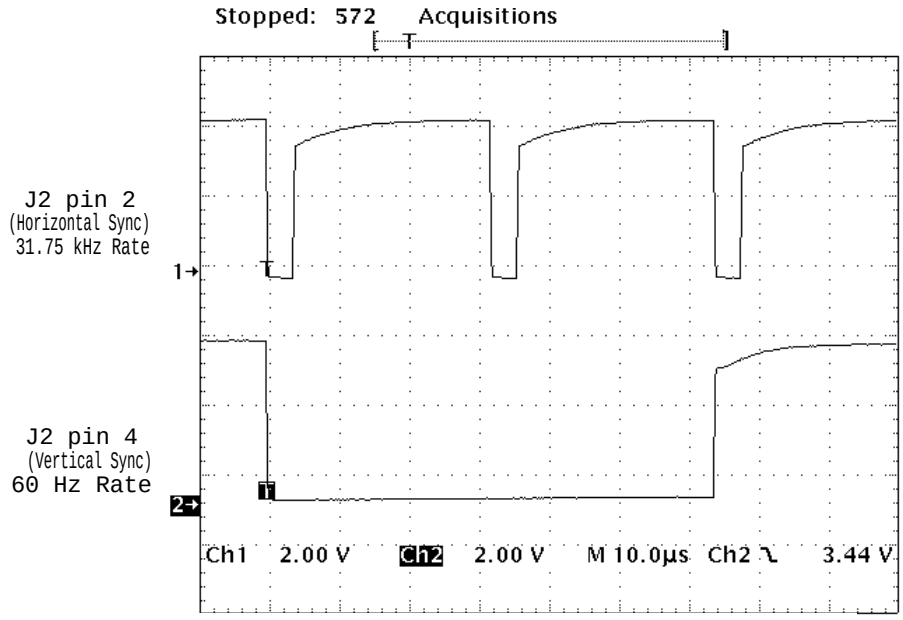


Figure 6-39: Horizontal and Vertical Sync Signals

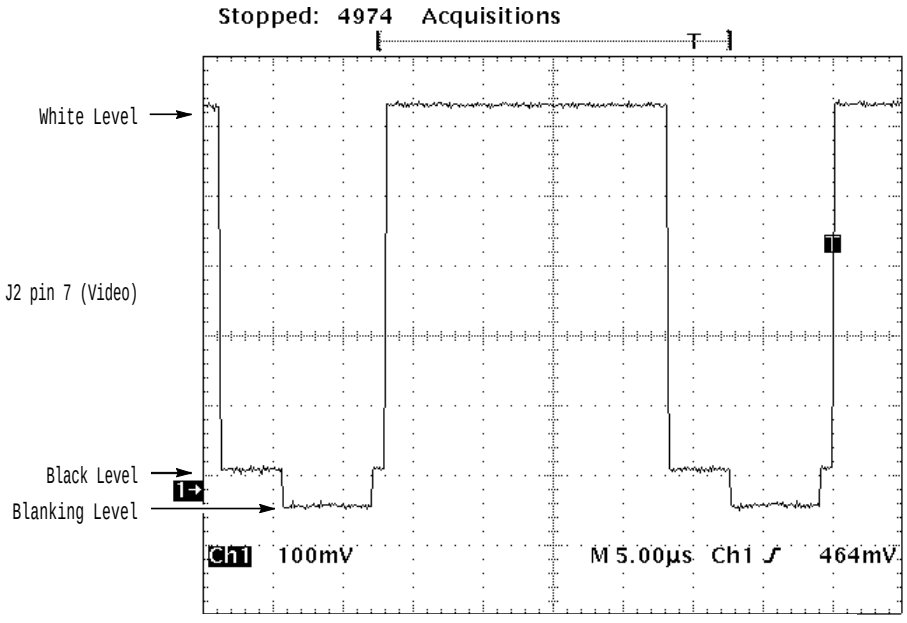


Figure 6-40: A Video Signal with White, Black, and Blanking

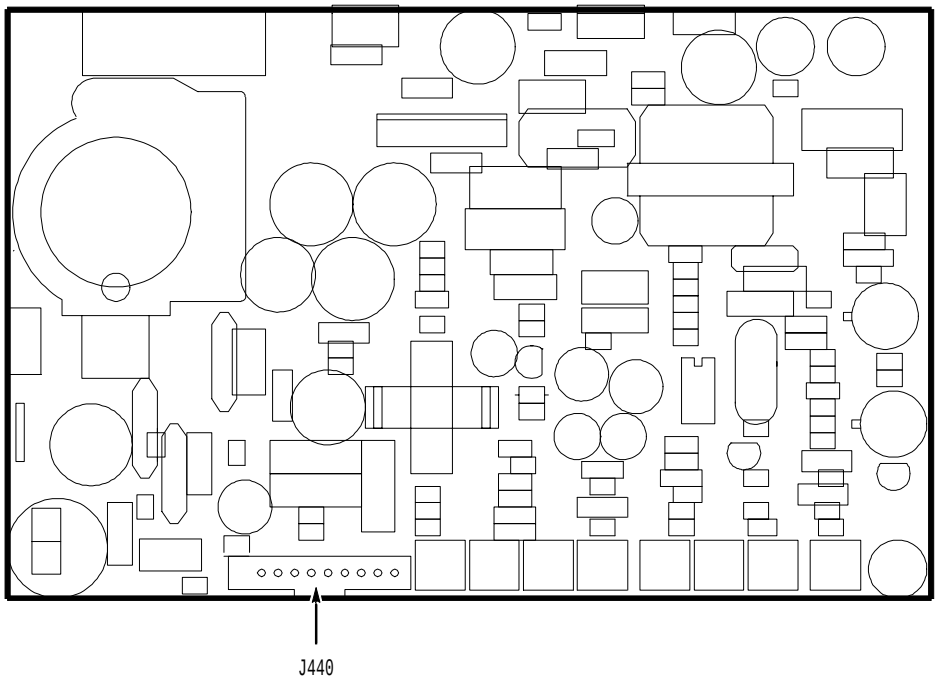


Figure 6-41: Monitor Connector J440

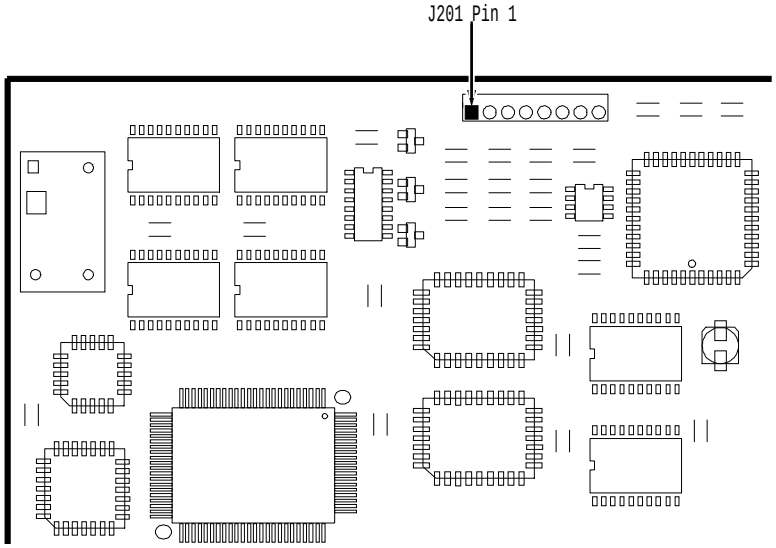


Figure 6-42: Display Connector J201

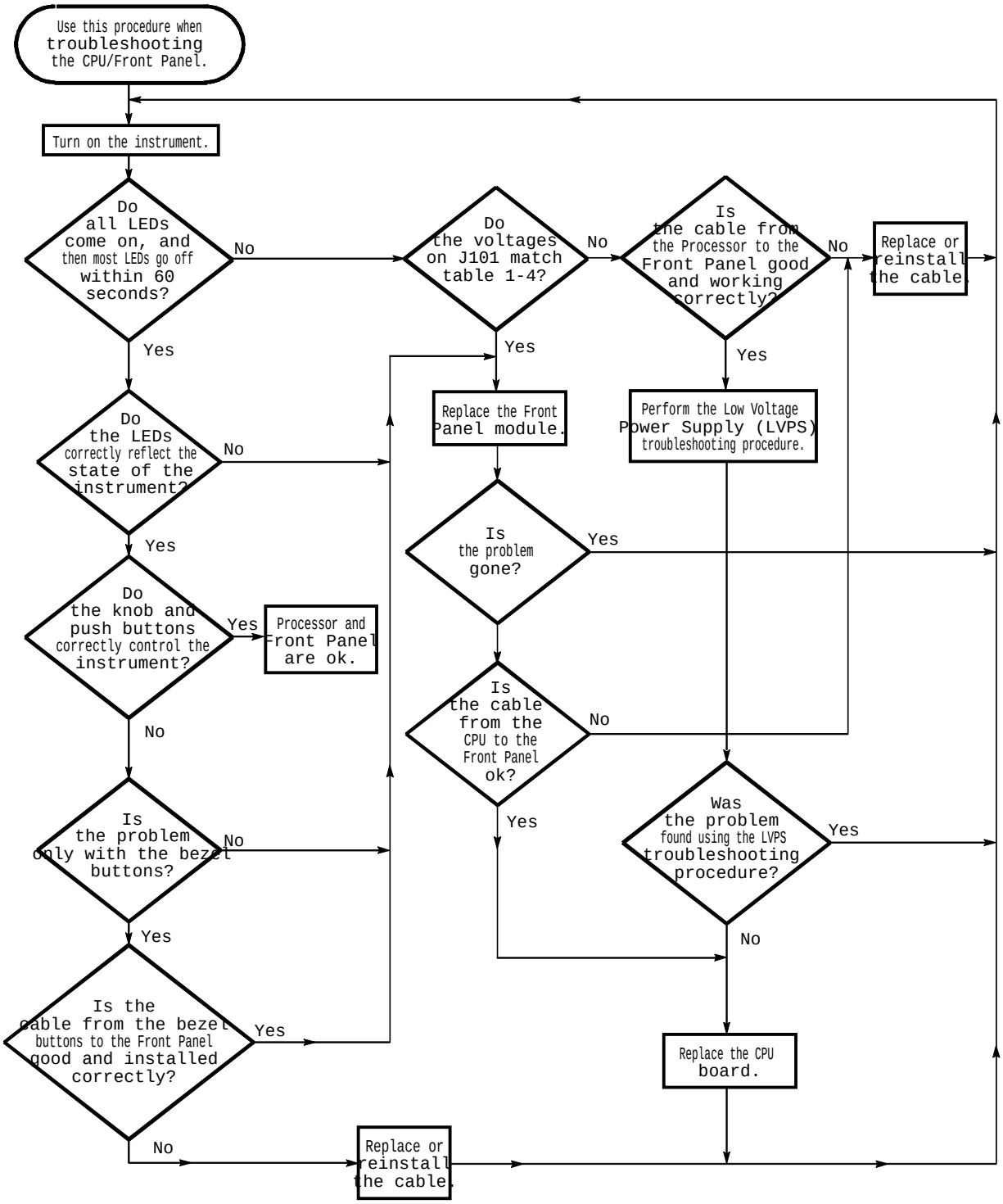


Figure 6-43: CPU/Front Panel Troubleshooting Procedure

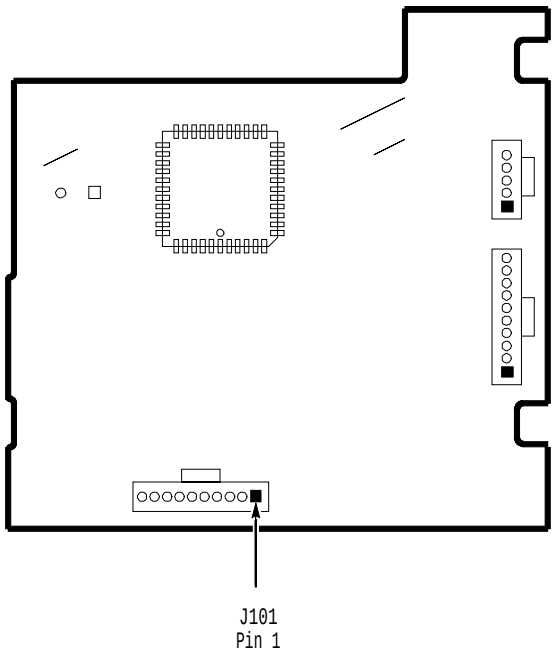


Figure 6-44: Front Panel Board Power Connector J101

Table 6-10: Front Panel Connector Voltages

Connector	Pin	Nominal Voltage
J101	Pins 2 and 4	5.1 V

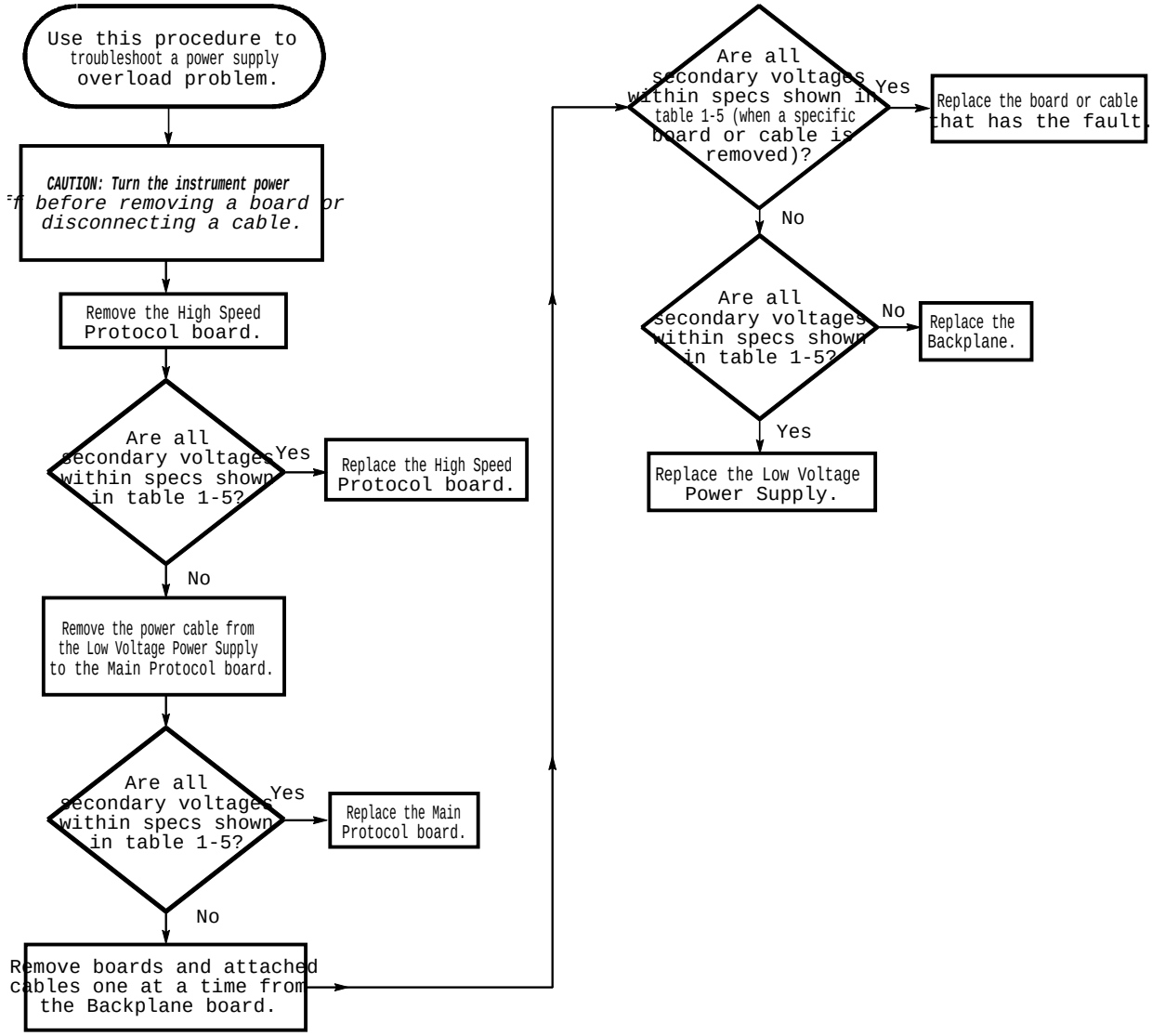


Figure 6-45: Low Voltage Power Supply Overload Troubleshooting Procedure

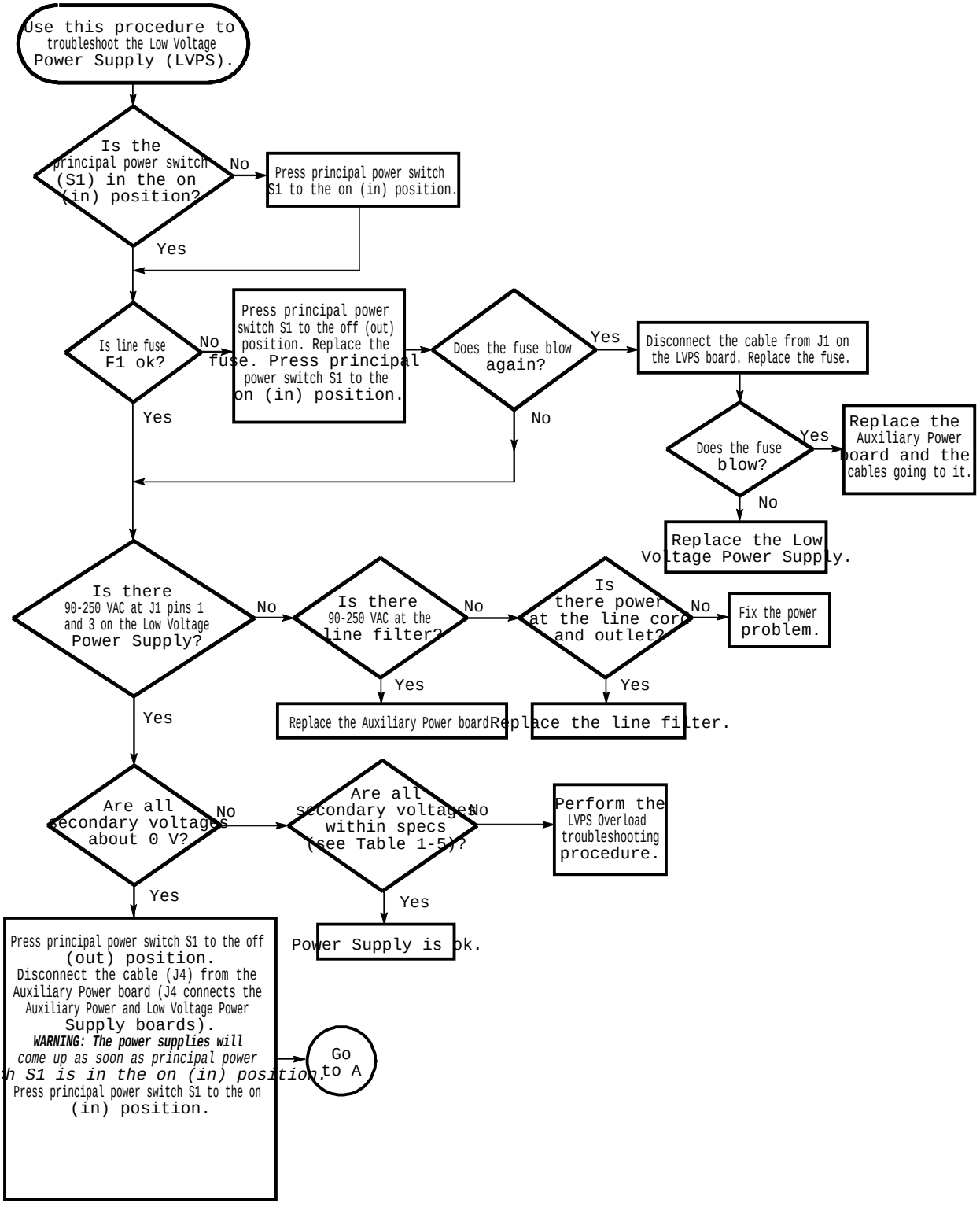


Figure 6-46: Low Voltage Power Supply Troubleshooting Procedure

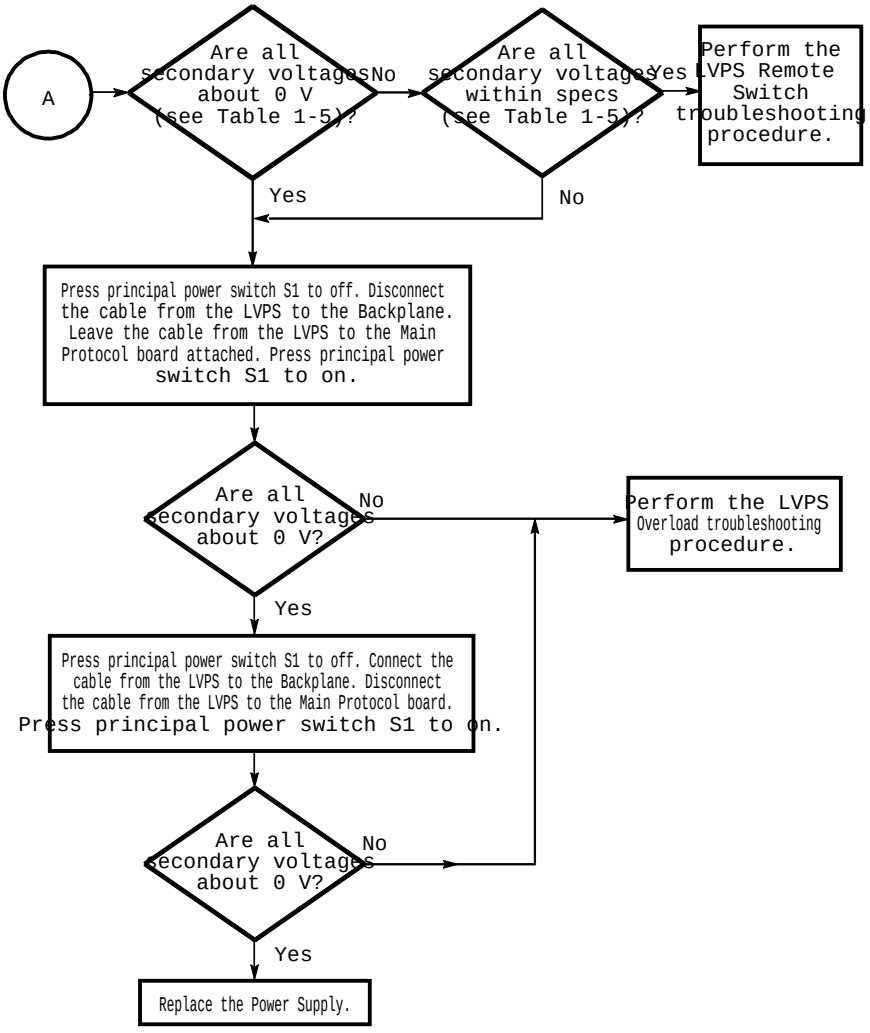


Figure 6-47: Low Voltage Power Supply Troubleshooting Procedure (Cont.)

Table 6-11: Normal Secondary Voltages

Supply	J15 Pin	Minimum Output	Maximum Output
+5.1 V	7	+5.05 V	+5.15 V
+15 V	3	+14.85 V	+15.15 V
-6.4 V	5	-6.35 V	-6.45 V
-15 V	1	-14.85 V	-15.15 V

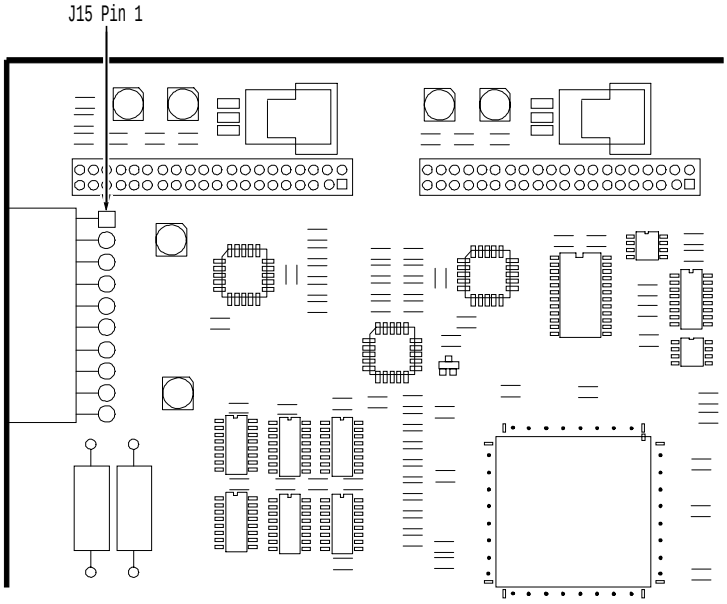


Figure 6-48: Main Protocol Board

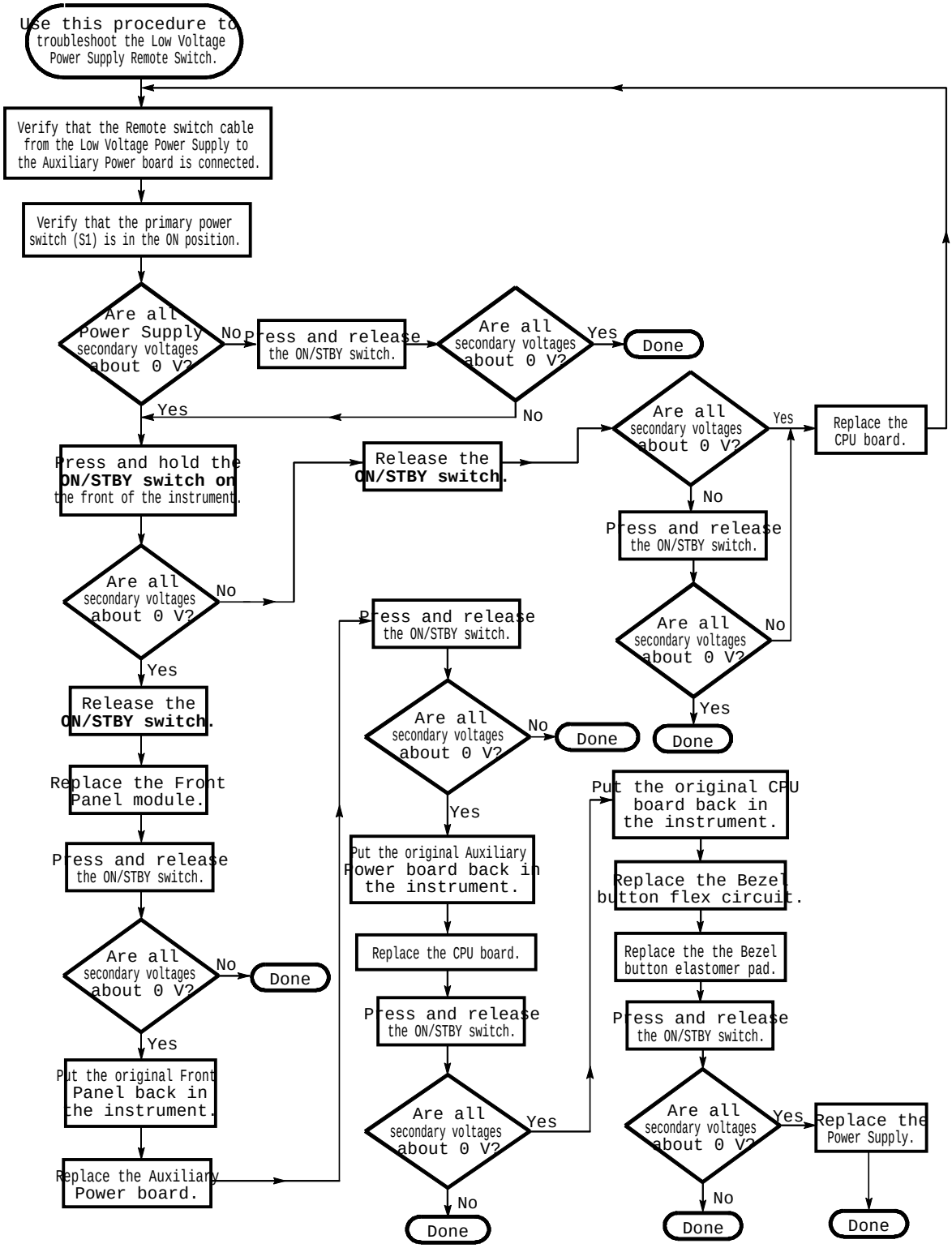


Figure 6-49: Low Voltage Power Supply Remote Switch Troubleshooting Procedure

Shared Routines

There are several routines that are shared by the diagnostic tests. Although you cannot invoke these shared routines individually, you might encounter error messages that originate with the shared routines. The following entries describe the shared routines.

RAM Data Line Routine

This general routine is used by various tests. The routine performs a walking–1's exercise on the specified memory location.

`Error Messages.` Potential error messages are as follows:

Test FAIL:

```
Addr: 0xXXXXXX, Exp: 0xXX, Act: 0xXX
```

The "Addr" field contains the address where the fault was detected. The "Exp" field contains the expected value and the "Act" field contains the actual data read from memory.

RAM Address/Data Routine

This general routine is used by various tests. The routine performs an address line/data pattern verification on the specified band of memory.

`Error Messages.`

Test FAIL:

```
Addr: 0xXXXXXX, Exp: 0xXX, Act: 0xXX
```

The "Addr" field contains the address where the fault was detected. The "Exp" field contains the expected value and the "Act" field contains the actual data read from memory.

Bus Errors Routine

This section describes the error messages produced due to a bus error during diagnostics.

When diagnostics are invoked, the diagnostics system swaps in its own bus error interrupt handler to trap any bus faults that may occur while testing. The diagnostic version of the bus error handler performs the following steps upon detecting a bus fault:

- Records the address of the location where the bus fault occurred.
- Performs back–to–back reads of the Protocol Board STTX Identity Register.

- Determines if any delay should be performed and prints a message to the VxWorks console port if performing a delay.

The individual test routines do not necessarily know whether or not a bus error occurred. The tests simply run to completion. The diagnostic control program checks if a bus error occurred at the completion of each test. Then, if a bus error did occur the Error Message described below is produced. The occurrence of a bus fault takes higher precedence than a test failure (since the bus error may be the source of the failure). Therefore if a test fails and a bus error occurred during the test, the diagnostics system will only report the error message describing the bus error.

The STTX Identity register on the protocol board contains information on the presence (or absence) of the various clocks. If a bus error occurred due to protocol hardware, this information may be useful. Therefore the diagnostic error message reports the contents of this register.

`Error Messages.` Potential error messages are as follows:

```
BUS ERROR At Addr: 0xXXXXXX, (STTX Reg 3: 0xXX)
```

Verify ADC (channel, minVal, maxVal) Routine

The “Addr” field contains the address where the bus fault occurred. The “STTX Reg 3” field contains the contents of the STTX Identity register.

This general routine is used to verify the output of a specified A/D channel falls within an allowed tolerance range. The exercise expects the following parameters:

- A/D Channel Number (0-7)
- Minimum Limit (mV)
- Maximum Limit (mV)

The exercise attempts to correct for errors in the A/D circuitry by also digitizing the ground and +2.5 V reference signals.

`Error Messages.` Potential error messages are as follows:

Test FAIL - A/D Completion:

The following error message is produced if the A/D converter fails to complete within the expected duration. The “Addr” and “Exp” fields define the register address and bit position of the A/D completion status bit.

```
Addr: 0x9B0000, Exp: 0x8000, Act: 0x0
```

Test FAIL - Limits:

The following error message is produced if the digitized signal does not fall within the allowed tolerance range. All values are reported in mV.

```
Min: X, Max: X, Act: X
```

loopbackHwInit() Routine

This routine places the protocol hardware in a quiescent state from which all loopback tests begin.

Error Messages. None.

This routine provides the main exercise of the protocol hardware. The routine programs the transmitter and receiver identically, then verifies the hardware is running error–free (no failures/alarms/errors). The routine assumes the loopback connection was made (either externally or internally) prior to invoking this routine. Once the integrity of the loopback path is checked, the test then verifies the hardware's ability to generate and detect various error conditions (single BIP errors and pointer movements).

loopbackTest (rate, type) Routine

The routine expects the following parameters:

- Line Rate (STS–1, STS–3, STS–12)
- Type (Electrical, Optical)

The routine exercises all possible structure/channel combinations for the specified rate.

Notes. Not indicated in the above description is how the test runs when invoked as part of the Self Test suite. To speed things up during self test, the exercise is not as exhaustive. The rate/structure/channel combinations exercised as part of self test are:

- 52Mb, STM-0 Structure, Channel 1
- 155Mb, STM-1 Structure, Channel 1
- 622Mb, STM-4 Structure, Channels 1-4

Error Messages. Potential error messages are as follows:

Test FAIL:

The following error message is produced if the hardware reports an unexpected failure, alarm, or error condition. The "Exp" field will be 0 if the test was checking for an error–free state. During the error insertion portion of the routine the field indicates the number of expected errors. The "Act" field indicates the number of errors reported by the hardware. For failures/alarms this value is 1. For errors, however, the value is a count read from the hardware.

<RATE_ID> <HW_STATUS>, Exp: 0xX, Act: 0xX

Where <RATE_ID>:
" Elec 52Mb" , " Elec 155Mb" , " Elec 622 Mb" ,
" Opt 52Mb" , " Opt 155Mb" , " Opt 622 Mb" ,
" Elec 52Mb (c)" , " Elec 155Mb (c)" ,
" Elec 622Mb (c)" ,
" Opt 52Mb (c)" , " Opt 155Mb (c)" ,
" Opt 622Mb (c)"

[(c) indicates concatenated structure]

Where <HW_STATUS>:
" LOS" , " LOF" , " LOP" ,
" (L/MS) AIS Alarm" , " PAIS Alarm" ,
" (L/MS) FERF Alarm" , " PFERF Alarm" ,
" Pattern Loss" ,
" B1 Error" , " B2 Error" , " B3 Error" ,
" Path FEBE Error" , " Payload Error" ,
" SPE/AU Pos Ptr Adj" , " SPE/AU Neg Ptr Adj"

Ex:
Opt 52Mb LOP, Exp: 0x0, Act: 0x1

The instrument was running at optical 52Mb rate, STS–1 structure and detected a LOP condition.

Tributary Shared Routines

There are several routines that are shared by tributary diagnostic tests. Although you cannot invoke these shared routines individually, you might encounter error messages that originate with the shared routines. The following entries describe the shared routines.

tribInit()

This routine is responsible for initializing the tributary board; including loading either the DSn/En XILINX.

`Error Messages.` Potential error messages are as follows:

Test FAIL - tribInit():

The following error message is produced if the tributary hardware load XILINX failed for either the DSn or En rate.

```
Load XILINX failure, Exp: 0x0, Act: 0x1
```

protoInit()

This routine is responsible for initializing both the tributary board and the protocol board. The initialization of the tributary board is performed by calling tribInit().

The routine initializes both the tributary board and the protocol board. After the initialization is complete, the tributary board is then connected to the Com Bus.

`Error Messages.` Potential error messages are as follows:

Test FAIL - protoInit():

The following error message is produced if the protocol hardware failed to initialize properly. A LOS, LOF, or LOP is present at the protocol loopback. This can be due to an STTX failure.

```
Elec 52Mb LOS/LOF/LOP, Exp: 0x0, Act: 0x1
```

The following error message is produced if the ADMA failed to initialize without any DS1 BIT errors.

```
ADMA failed to initialize, Exp: 0x0, Act: 0x1
```

diagGroup TestSet (Tributary Rate)

This routine provides the main exercise for the tributary hardware test set. This is accomplished by looping the test set transmitter to its receiver. Both the mapper/demapper and line interface are disconnected during this test.

To test the ability of the test set to generate and receive various DSn/En alarms (AIS, YELLOW, REMOTE), the routine loops through all the available DSn/En alarms and verify that each of these can be transmitted and received.

To verify that the test set can generate and receive various DSn/En errors (BIT, FRAME, CRC, C–Bit, P–Bit), the routine loops through all the available DSn/En errors and verifies that each of these can be transmitted and received.

To test the various DSn/En framing formats (UNFRAMED, SF, ESF, C–BIT, M13, PCM30, PCM31, PCM30CRC, PCM31CRC, FRAMED), the routine programs the transmitter and receiver identically, then verifies that the hardware is running error–free (no failures/alarms/errors). Once the integrity of the loopback path is checked, the test then verifies the ability of the test set to generate and detect pattern bit errors.

To verify the ability of the test set to generate and receive a DSn/En pattern (PRBS23), the routine first programs the transmitter and receiver to the same pattern. It then verifies that pattern lock is present. Finally, the receiver is then programmed to a different pattern, and it then verifies that pattern lock is not present. The routine expects the following parameters: diagGroupTestSet (DS1, DS3, E1, E3).

The routine exercises the ability of the tributary hardware to generate and receive DSn/En alarms, errors, framing formats, and patterns.

`Error Messages.` Potential error messages are as follows:

Test FAIL - Initialization:

Refer to *tribInit*, on page -4, for a list of possible error messages during initialization.

Test FAIL - diagTribTestSetAlarms():

The following error message is produced if the hardware expected to see a specific DSn/En alarm, but the alarm was not present.

```
<ALARM>, Exp: 0x1, Act: 0x0

     Where <ALARM>:
          " AIS" , " Yellow" ,
" Remote" ,
```

The following error message is produced if the hardware expected to see no alarms, but instead a DSn/En alarm is present.

```
<ALARM>, Exp: 0x0, Act: 0x1
```

```
                Where <ALARM>:
                      " AIS" , " Yellow" ,
" Remote"
```

Test FAIL - diagTribTestSetErrors():

The following error message is produced if the number of DSn/En errors inserted does not equal the number of DSn/En errors detected. The "Act" field indicates the number of errors reported by the hardware. The "Exp" field indicates the number of errors expected.

```
      <ERROR>, Exp: 0xX, Act: 0xX

            Where <ERROR>:
                  " Bit" , " Frame" , " CRC" ,
" CBIT CP" , " P-Bit" ,
```

Test FAIL - diagTribTestSetFraming():

The following error message is produced if the hardware expected to see no alarms, but instead a DSn/En alarm is present.

```
<FRAMING FORMAT>, <ALARM>, Exp: 0x0, Act:
0x01

      Where <FRAMING FORMAT>:
            " Unframed" , " Super Frame" ,
            " Ext. Super Frame" , " C Bit" ,
" M13" ,
            " PCM30" , " PCM31" , " PCM30 CRC" ,
            " PCM31 CRC" , " Framed"

      Where <ALARM>:
            " AIS" , " Yellow" , " Remote"
```

The following error message is produced if the hardware expected to see no DSn/En errors, but instead a DSn/En error is present. The "Act" field indicates the number of errors reported by the hardware.

```
<FRAMING FORMAT>, <ERROR>, Exp: 0x0, Act: 0xX

      Where <FRAMING FORMAT>:
            " Unframed" , " Super Frame" ,
            " Ext. Super Frame" , " C Bit" ,
" M13" ,
            " PCM30" , " PCM31" , " PCM30 CRC" ,
            " PCM31 CRC" , " Framed"

      Where <ERROR>:
            " Bit" , " Frame" , " CRC" , " CBIT
CP" , " P-Bit"
```

The following error message is produced if the number of DSn/En BIT errors inserted does not equal the number of DSn/En BIT errors detected. The “Act” field indicates the number of DSn/En BIT errors reported by the hardware. The “Exp” field indicates the number of DSn/En BIT errors expected.

```
<FRAMING FORMAT>, <Bit>, Exp: 0x0, Act: 0xX

     Where <FRAMING FORMAT>:
          “ Unframed” , “ Super Frame” ,
          “ Ext. Super Frame” , “ C Bit” ,
“ M13” ,
          “ PCM30” , “ PCM31” , “ PCM30 CRC” ,
          “ PCM31 CRC” , “ Framed”
```

Test FAIL - diagTribTestSetPatterns():

The following error message is produced if the hardware expected to see a pattern lock, but no pattern lock was present.

```
TX/RX Pat: PRBS23, Pat. Lock, Exp: 0x1, Act:
0x0
```

The following error message is produced if the hardware expected to see no pattern lock, but a pattern lock was present.

```
Tx/Rx Pat: Diff., Pat. Lock, Exp: 0x0, Act:
0x1
```

diagGroupLineInterace (Tributary Rate Loopback)

This routine tests the connection between the test set and the line interface. This is accomplished by connecting the test set to the line interface through the configuration switch. The mapper/demapper is disconnected during this test.

To test the ability of the line interface to detect an LOS condition, the routine first programs the transmitter and receiver identically. It then verifies that a valid DSn/En signal is received. Finally, the connection between the test set and line interface is broken, and it then verifies that an LOS condition is present.

To test the various line codings, the routine programs the transmitter and receiver identically, then verifies the hardware is running error free (no failures/alarms/errors). Once the integrity of the loopback path is checked, the test then verifies the ability of the hardware to generate and detect pattern bit errors. The routine diagGroupLineInterface expects the following parameters: Tributary Rate (DS1, DS3, E1, E3, E4)loopback (Internal, External).

The routine tests the ability of the line interface to detect an LOS, and its ability to generate and receive all possible line coding formats.

`Error Messages.` Potential error messages are as follows:

Test FAIL - Initialization:

Refer to *tribInit*, on page -4, for a list of possible error messages during initialization.

Test FAIL - diagLineInterfaceLos():

The following error message is produced if the hardware expected to see a DSn/En signal, but a LOS was detected.

```
LOS, Exp: 0x0, Act: 0x1
```

The following error message is produced if the hardware expected to see a LOS status, but a valid DSn/En signal was detected.

```
LOS, Exp: 0x1, Act: 0x0
```

Test FAIL - diagLineInterfaceCode():

The following error message is produced if the hardware expected to see no alarms, but a DSn/En alarm is present.

```
<LINE_CODING>, <ALARM>, Exp: 0x0, Act: 0x1

     Where <LINE_CODING>:
          " AMI" , " B8ZS" , " HDB3" ,
" B3ZS" , " CMI"

     Where <ALARM>:
          " AIS" , " Yellow" , " Remote"
```

The following error message is produced if the hardware expected to see no errors, but a DSn/En error is present. The "Act" field indicates the number of errors reported by the hardware.

```
<LINE_CODING>, <ERROR>, Exp: 0x0, Act: 0xX

     Where <LINE_CODING>:
          " AMI" , " B8ZS" , " HDB3" ,
" B3ZS" , " CMI"

     Where <ERROR>:
          " Bit" , " Frame" , " CRC" , " CBIT
CP" , " P-BIT" ,
```

The following error message is produced if the number of DSn/En BIT errors inserted does not equal the number of DSn/En BIT errors detected. The “Act” field indicates the number of bit errors reported by the hardware. The “Exp” field indicates the number of bit errors expected.

```
<LINE_CODING>, >ERROR>, Exp: 0xX, Act: 0xX

     Where <LINE_CODING>:
          “ AMI” , “ B8ZS” , “ HDB3” ,
“ B3ZS” , “ CMI”

     Where <ERROR>:
          “ Bit” , “ Frame” , “ CRC” , “ CBIT
CP” , “ P-BIT”
```

diagGroupMapDemap (Tributary Rate)

This routine tests the connection between the test set and the mapper/demapper. This is accomplished by connecting the test set to the mapper/demapper through the configuration switch. The line interface is disconnected during this test.

To test the ability of the mapper/demapper to generate and receive various VT/TU alarms and failures (VT AIS, VT YELLOW, VT LOP, VT LOM), the routine loops through all the available VT/TU alarms and failures and verifies that each of these can be transmitted and received.

To verify that the mapper/demapper can generate and receive various VT/TU errors (VT BIP, VT FEBE), the routine loops through all the available VT/TU errors and verifies that they can be transmitted and received.

To test the ability of the mapper/demapper to switch between active VT/TU channels, the routine programs the transmitter and receiver to the same active VT/TU channels. Then the test verifies that the mapper/demapper can transmit and detect VT/TU BIP errors.

To verify that the mapper/demapper can generate background VT/TU patterns, the routine programs the active VT/TU channel to contain a PRBS23 pattern and the inactive VT/TU channel to a different pattern (QRSS or PRBS15). The receiver is then set to the active VT/TU channel and a pattern lock is verified with a PRBS23 pattern. Finally, the receiver is set to the inactive VT/TU channel and a pattern lock is verified for either a QRSS or PRBS15 pattern (depending on the DSn/En rate).

To verify that the mapper/demapper can generate background VT/TU framing formats, the routine programs the active and inactive VT/TU channel to a set framing format. Then the routine switches the receiver between the active and inactive VT/TU channels and verifies that the expected framing format is present. For VT channels, the active channel framing format is set to unframed and the inactive VT channel framing format is set to extended super frame. For TU

channels, the active and inactive channel framing formats are set to PCM30CRC (TU-12) or framed (TU-3).

Finally, the routine also verifies that the mapper/demapper can map and demap DSn/En alarms and errors. To do this, the transmitter and receiver are programmed identically. The integrity of the loopback is verified by checking for a pattern lock. Then the test generates DSn/En errors and alarms. The routine expects the following parameters: (DS1, DS3, E1, E3, E4).

The routine exercises the ability of the tributary hardware to map/demap DSn/En signals. The test generates and receives VT/TU alarms, failures, errors, framing formats, and patterns.

Error Messages. Potential error messages are as follows:

Test FAIL - Initialization():

Refer to protoInit, on page -5, for a list of possible error messages during initialization.

Test FAIL - diagTribMapDemapFailures():

The following error message is produced if the hardware expected no VT/TU failures, but a VT/TU failure is present.

```
<FAILURE>, Exp: 0x0, Act: 0x1

     Where <FAILURE>:
          " VT LOP" , " VT LOM"
```

The following error message is produced if the hardware expected a specific VT/TU failure, but the failure was not present.

```
<FAILURE>, Exp: 0x1, Act: 0x0

     Where <FAILURE>:
          " VT LOP" , " VT LOM"
```

Test FAIL - diagTribMapDemapAlarms():

The following error message is produced if the hardware expected no VT/TU alarms, but instead a VT/TU alarm is present.

```
<ALARM>, Exp: 0x0, Act: 0x1

     Where <ALARM>:
          " VT AIS" , " VT Yellow"
```

The following error message is produced if the hardware expected a specific VT/TU alarm, but the alarm was not present.

```
<ALARM>, Exp: 0x1, Act: 0x0

     Where <ALARM>:
          " VT AIS" , " VT Yellow"
```

Test FAIL - diagTribMapDemapErrors():

The following error message is produced if the number of VT/TU errors inserted does not equal the number of VT/TU errors detected. The “Act” field indicates the number of errors reported by the hardware. The “Exp” field indicates the number of errors expected.

```
<ERROR>, Exp: 0xX, Act: 0xX

     Where <ERROR>:
          “ VT BIP” , “ VT FEBE”
```

Test FAIL - diagTribMapDemapChannels():

The following error message is produced if the number VT/TU BIP errors inserted does not equal the number of VT/TU BIP errors detected. The “Act” field indicates the number of errors reported by the hardware. The “Exp” field indicates the number of errors expected.

```
VT BIP, Exp: 0xX, Act: 0xX
```

Test FAIL - diagTribMapDemapBckgndData():

The following error message is produced if the hardware expected a pattern lock on either the active channel or background channel, but no pattern lock was present.

```
<CHANNEL>, Pattern Lock, Exp: 0x1, Act: 0x0
     Where <CHANNEL>:
          “ Act Ch.” , “ Bckgnd Ch.”
```

Test FAIL - diagTribMapDemapBckgndFraming():

The following error message is produced if the hardware expected no VT/TU errors, but a VT/TU error is present. The “Act” field indicates the number of errors reported by the hardware.

```
<FRAMING FORMAT>, <ERROR>, Exp: 0x0, Act: 0xX
     Where <FRAMING FORMAT>
          “ Unframed” , “ Ext. Super Frame” ,
          “ PCM30 CRC” , “ Framed”

     Where <ERROR>
          “ VT BIP” , “ VT FEBE”
```

Test FAIL - diagTribMapDemapTestSet():

The following error message is produced if the hardware expected a pattern lock, but no pattern lock was present.

```
Pattern Lock, Exp: 0x1, Act: 0x0
```

The following error message is produced if the number of DSn/En errors inserted does not equal the number of DSn/En errors detected. The “Act” field indicates the number of errors reported by the hardware. The “Exp” field indicates the number of errors expected.

```
<ERROR>, Exp: 0xX, Act: 0xX
     Where <ERROR>
          “ Bit” , “ Frame”
```

The following error message is produced if the hardware expected an E4 AIS alarm, but the alarm was not present.

```
AIS, Exp: 0x1, Act: 0x0
```

diagTribRing (Tributary Rate)

This routine verifies the overall operation of the tributary board by connecting all the major tributary hardware blocks (test set, mapper/demapper, and line interface) through the configuration switch. Once all the blocks are connected, various VT/TU and DSn/En alarms, errors, and failures are tested. The routine expects the following parameters: diagTribRing (DS1, DS3, E1, E3, E4).

The routine tests the ability of the tributary hardware to generate and receive VT/TU and DSn/En alarms, errors, and failures.

Error Messages. Potential error messages are as follows:

Test FAIL - diagTribRing():

The following error message is produced if the hardware expected a pattern lock, but instead no pattern lock was present.

```
Pattern Lock, Exp: 0x1, Act: 0x0
```

The following error message is produced if the number of DSn/En BIT errors inserted does not equal the number of DSn/En BIT errors detected. The “Act” field indicates the number of BIT errors reported by the hardware. The “Exp” field indicates the number of BIT errors expected.

```
Bit, Exp: 0xX, Act: 0xX
```

The following error message is produced if the hardware expected a DSn/En AIS alarm, but the alarm was not present.

```
AIS, Exp: 0x1, Act: 0x0
```

The following error message is produced if the hardware expected no DSn/En alarms, but a DSn/En alarm is present.

```
<ALARM>, Exp: 0x0, Act: 0x1

     Where <ALARM>:
          “ AIS” , “ Yellow” , “ Remote”
```

The following error message is produced if the hardware expected no VT/TU alarms, but a VT/TU alarm is present.

```
<ALARM>, Exp: 0x0, Act: 0x1

     Where <ALARM>:
          " VT AIS" , " VT Yellow"
```

The following error message is produced if the hardware expected no VT/TU failures, but a VT/TU failure is present.

```
<FAILURE>, Exp: 0x0, Act: 0x1

     Where <FAILURE>:
          " VT LOP" , " VT LOM"
```

The following error message is produced if the hardware expected a VT/TU Yellow alarm, but the alarm was not present.

```
VT Yellow, Exp: 0x1, Act: 0x0
```

The following error message is produced if the number of VT/TU BIP errors inserted does not equal the number of VT/TU BIP errors detected. The "Act" field indicates the number of errors reported by the hardware. The "Exp" field indicates the number of errors expected.

```
VT BIP, Exp: 0xX, Act: 0xX
```

Diagnostic Test Descriptions

The following diagnostic test descriptions include the name of the test, a short description, a command line which can be used to invoke the test via GPIB, and a list of error messages that the test can generate. Table 7-6 summarizes the diagnostic tests available.

Table 6-12: Diagnostic Test Summary

Test Group	Tests		
Self Test (Power–Up)	Refer to Table 6-2 for a list of all tests		
System Internal	Refer to Table 6-3 for a list of all tests		
System External	Refer to Table 6-4 for a list of all tests		
Protocol	Misc Register SETI Register Register Access Flash Voltage Flash Checksum	ITX RAM IRX RAM PRX RAM IRX FIFO A/D Converter	Power Supply 52Mb Loop 155Mb Loop 622Mb Loop VC4-4C
Clock	Internal Reference Freq Offset		
O/E Module	Status Identification Access Tx Optical Power	Rx Signal Level Internal 52Mb Loop Internal 155Mb Loop Internal 622Mb Loop	External 52Mb Loop External 155Mb Loop External 622Mb Loop
Tributary	Trib Flash Voltage Trib Flash Checksum 2 Mb Ring 34 Mb Ring Trib E1 Test Set Trib E2 Test Set Trib E3 Test Set Trib E4 Test Set Trib E1 Line Interface (Internal) Trib E2 Line Interface (Internal) Trib E3 Line Interface (Internal)	Trib E4 Line Interface (Internal) Trib E1 Line Interface (External) Trib E2 Line Interface (External) Trib E3 Line Interface (External) Trib E4 Line Interface (External) Trib E1 Map & Demap Trib E3 Map & Demap Trib E4 Map & Demap Mux/Demux E1 Chan	Mux/Demux E2 Chan Mux/Demux E3 Chan Mux/Demux E1 Patt Mux/Demux E2 Patt Mux/Demux E3 Patt Trib M45 Test Set 45 Mb Ring Trib M45 Line Interface (Internal) Trib M45 Line Interface (External) Trib M45 Map & Demap Trib E1 Unbalanced Line Interface (External)
JAWA	Clock Recovery Circuit Register Access Flash Checksum DAC Loopback	Clock Recovery Divider Tracking PLL Meas Phase Detector	Meas PLL Gain FIFO Analog Output

		Meas PLL Locking	
JAWG	Wander Loop Locking Jitter Loop Locking	Jitter Loop Low–Pass Filters	Jitter Generation
CPU	Vector Interrupt IIC Control Clock/Calendar	Clk/Cal Battery DUART	
Display	Video RAM RAMDAC White Field	Grey Field White Box Test Grid	Composite HW Scrolling
Front Panel	Internal (Front Panel Self Test) LEDs	Speaker Manual (Interactive)	
Disk	PM110 Register PM110 Cache PM110 Counter	Controller Drive Format & Verify	Dysan Seek

Self Test

The Self Test group refers to the suite of tests that are invoked as part of the power–up process. These test routines are designed to verify the maximum amount of hardware in the minimum amount of time. The group provides thorough coverage of the hardware, but offers very little in the way of fault isolation.

The Self Test group is useful for catching intermittent power–up failures. If the instrument occasionally fails power–up diagnostics, it may be useful to loop on the Self Test diagnostics to verify the failure occurs. If a failure is then detected, it is recommended that the appropriate board–level suite of tests be invoked to aid in the fault isolation process. The first word of each failure message identifies the test group with which the routine is associated (e.g. Proto, O/E, etc.).

GPIB Command. *TST?

Table 6-13 lists the tests along with their corresponding test numbers that are invoked as part of the Self Test suite.

Table 6-13: Self Test Summary

Test Name	Test Number	Board (FRU)
CPU Vector Interrupt	1	Processor Board
CPU IIC Control	2	Processor Board
CPU Clock/Calendar	3	Processor Board
CPU Float Pt (68881)	4	Processor Board
CPU DUART	5	Processor Board
Proto Flash Voltage	28	Protocol Board
Proto Flash Chksum	29	Protocol Board
Proto Power Supply	35	Protocol Board
Trib Flash Checksum	54	Tributary
Trib Ring E1	86	Tributary
Trib Ring E3	87	Tributary
Trib Ring M45	88	Tributary
Jit Flash Checksum	96	JAWA/JAWG

Error Messages. See the individual test descriptions for the explanation of possible failures.

System Internal Test

The System Internal group is similar to the Self Test group in that it is a collection of various tests, not just those specific to a single board. This group includes all tests that do not require user interaction or external cabling.

The purpose of the System Internal group is to provide a convenient way of running all internal diagnostics with a single command. This suite of tests is more thorough than the self test group and provides an exhaustive exercise of the instrument. By running this test group and verifying no faults were detected, the user should have a high level of confidence in the integrity of the instrument.

Table 6-14 lists the tests along with their corresponding test numbers that are invoked as part of the System Internal group.

Table 6-14: System Internal Diagnostic Test Summary

Test Name	Test Number	Board (FRU)
CPU Vector Interrupt	1	Processor Board
CPU IIC Control	2	Processor Board
CPU Clock/Calendar	3	Processor Board
CPU Float Pt (68881)	4	Processor Board
CPU DUART	5	Processor Board
Display Video RAM	6	Display Board
Display RAMDAC	7	Display Board
Disk PM110 Reg Test	14	Disk Drive
Disk PM110 Cache RAM	15	Disk Drive
Disk PM110 Counter	16	Disk Drive
Disk Controller	17	Disk Drive
Disk Drive	18	Disk Drive
Proto Misc Reg	25	Protocol Board
Proto SETI Reg	26	Protocol Board
Proto Reg Access	27	Protocol Board
Proto Flash Voltage	28	Protocol Board
Proto Flash Chksum	29	Protocol Board
Proto ITX RAM	30	Protocol Board
Proto IRX RAM	31	Protocol Board
Proto PRX RAM	32	Protocol Board
Proto IRX FIFO	33	Protocol Board
Proto A/D Conv.	34	Protocol Board
Proto Pwr Supply	35	Protocol Board
Proto Bd 52Mb Loop	36	Protocol Board

Proto Bd 155Mb Loop	37	Protocol Board
Proto Bd 622Mb Loop	38	Protocol Board
Proto Bd STM4C	39	Protocol Board
Clk Internal Ref	40	Clock Board
Clk Freq Offset	41	Clock Board
O/E Status	42	Plug–In Interface Module
O/E Identification	43	Plug–In Interface Module
O/E Access	44	Plug–In Interface Module
O/E Tx Optical Power	45	Plug–In Interface Module
O/E Int 52 Mb Loop	47	Plug–In Interface Module
O/E Int 155 Mb Loop	48	Plug–In Interface Module
O/E Int 622 Mb Loop	49	Plug–In Interface Module
Trib Flash Voltage	53	Tributary
Trib Flash Checksum	54	Tributary
Trib Register Access	55	Tributary
Trib TestSet E1	58	Tributary
Trib TestSet E2	59	Tributary
Trib TestSet E3	60	Tributary
Trib TestSet 45 Mb/s	61	Tributary
Trib TestSet E4	62	Tributary
Trib Line Int E1	73	Tributary
Trib Line Int E2	74	Tributary
Trib Line Int E3	75	Tributary
Trib Line Int 45 Mb/s	76	Tributary
Trib Line Int E4	77	Tributary
Trib Map/Demap E1	80	Tributary

Trib Map/Demap E3	81	Tributary
Trib Map/Demap 45 Mb/s	82	Tributary
Trib Map/Demap E4	83	Tributary
Trib Ring E1	86	Tributary
Trib Ring E3	87	Tributary
Trib Ring M45	88	Tributary
Trib Mux/Dmx E1 Channel	89	Tributary
Trib Mux/Dmx E2 Channel	90	Tributary
Trib Mux/Dmx E3 Channel	91	Tributary

Trib Mux/Dmx E1 Pattern	92	Tributary
Trib Mux/Dmx E2 Pattern	93	Tributary
Trib Mux/Dmx E3 Pattern	94	Tributary
Jit Register Access	95	JAWA/JAWG
Jit Flash Checksum	96	JAWA/JAWG
Jit FIFO Test	97	JAWA/JAWG
Jit DAC Loopback	98	JAWA/JAWG
Jit Divider A	99	JAWA/JAWG
Jit Tracking PLL	100	JAWA/JAWG
Jit Clk Rec Cir E1	101	JAWA/JAWG
Jit Clk Rec Cir E2	102	JAWA/JAWG
Jit Clk Rec Cir E3	103	JAWA/JAWG
Jit Clk Rec Cir M45	104	JAWA/JAWG
Jit Clk Rec Cir E4STM1	105	JAWA/JAWG
Jit Clk Rec Cir STM0	106	JAWA/JAWG
Jit Clk Rec Cir STM4	107	JAWA/JAWG
Jit Tx Low–Pass Filter	108	JAWA/JAWG
Jit Wander Loop	109	JAWA/JAWG
Jit Jitter Loop	110	JAWA/JAWG
Jit Jitter Generation	111	JAWA/JAWG
Jit Phase Detector	112	JAWA/JAWG
Jit PLL Locking	113	JAWA/JAWG
Jit PLL Gain	114	JAWA/JAWG
Jit Analog Output	115	JAWA/JAWG

GPIB Command. DIAG:SELECT SYSINTERNAL

Error Messages. See the individual test descriptions for the explanation of possible failures.

System External Test

The System External group is a super set of the System Internal group. This test suite includes all of the same routines, plus additional tests that make use of external loopback cables.

As with the System Internal group, the purpose of the System External group is to provide the user a high level of confidence in the integrity of the hardware. By making use of external cables, the hardware is verified up to and including the connectors themselves.

Table 6-15 lists the tests along with their corresponding test numbers that are invoked as part of the System External group.

Table 6-15: System External Diagnostic Test Summary

Test Name	Test Number	Board (FRU)
CPU Vector Interrupt	1	Processor Board
CPU IIC Control	2	Processor Board
CPU Clock/Calendar	3	Processor Board
CPU Float Pt (68881)	4	Processor Board
CPU DUART	5	Processor Board
Display Video RAM	6	Display Board
Display RAMDAC	7	Display Board
Disk PM110 Reg Test	14	Disk Drive
Disk PM110 Cache RAM	15	Disk Drive
Disk PM110 Counter	16	Disk Drive
Disk Controller	17	Disk Drive
Disk Drive	18	Disk Drive
Proto Misc Reg	25	Protocol Board
Proto SETI Reg	26	Protocol Board
Proto Reg Access	27	Protocol Board
Proto Flash Voltage	28	Protocol Board
Proto Flash Chksum	29	Protocol Board
Proto ITX RAM	30	Protocol Board
Proto IRX RAM	31	Protocol Board
Proto PRX RAM	32	Protocol Board
Proto IRX FIFO	33	Protocol Board

Proto A/D Conv.	34	Protocol Board
Proto Pwr Supply	35	Protocol Board
Proto Bd 52Mb Loop	36	Protocol Board
Proto Bd 155Mb Loop	37	Protocol Board
Proto Bd 622Mb Loop	38	Protocol Board
Proto Bd STM4C	39	Protocol Board
Clk Internal Ref	40	Clock Board
Clk Freq Offset	41	Clock Board
O/E Status	42	Plug–In Interface Module
O/E Identification	43	Plug–In Interface Module
O/E Access	44	Plug–In Interface Module
O/E Tx Optical Power	45	Plug–In Interface Module
O/E Rx Signal Level	46	Plug–In Interface Module
O/E Ext 52 Mb Loop	50	Plug–In Interface Module
O/E Ext 155 Mb Loop	51	Plug–In Interface Module
O/E Ext 622 Mb Loop	52	Plug–In Interface Module
Trib Flash Voltage	53	Tributary
Trib Flash Checksum	54	Tributary
Trib Register Access	55	Tributary
Trib TestSet E1	58	Tributary
Trib TestSet E2	59	Tributary
Trib TestSet E3	60	Tributary
Trib TestSet 45 Mb/s	61	Tributary
Trib TestSet E4	62	Tributary
Trib Line Ext E1 Unbalanced	65	Tributary
Trib Line Ext E1 Balanced	66	Tributary
Trib Line Ext E2	67	Tributary

Trib Line Ext E3	68	Tributary
Trib Line Ext 45 Mb/s	69	
Trib Line Ext E4	70	Tributary
Trib Line Int E1	73	Tributary
Trib Line Int E2	74	Tributary
Trib Line Int E3	75	Tributary
Trib Line Int 45 Mb/s	76	Tributary
Trib Line Int E4	77	Tributary
Trib Map/Demap E1	80	Tributary
Trib Map/Demap E3	81	Tributary
Trib Map/Demap 45 Mb/s	82	Tributary
Trib Map/Demap E4	83	Tributary
Trib Ring E1	86	Tributary
Trib Ring E3	87	Tributary
Trib Ring M45	88	Tributary
Trib Mux/Dmx E1 Channel	89	Tributary
Trib Mux/Dmx E2 Channel	90	Tributary
Trib Mux/Dmx E3 Channel	91	Tributary
Trib Mux/Dmx E1 Pattern	92	Tributary
Trib Mux/Dmx E2 Pattern	93	Tributary
Trib Mux/Dmx E3 Pattern	94	Tributary
Jit Register Access	95	JAWA/JAWG
Jit Flash Checksum	96	JAWA/JAWG
Jit FIFO Test	97	JAWA/JAWG
Jit DAC Loopback	98	JAWA/JAWG
Jit Divider A	99	JAWA/JAWG
Jit Tracking PLL	100	JAWA/JAWG
Jit Clock Recovery	101	JAWA/JAWG

Cir E1		
Jit Clock Recovery Cir E2	102	JAWA/JAWG
Jit Clock Recovery Cir E3	103	JAWA/JAWG
Jit Clock Recovery Cir M45	104	JAWA/JAWG
Jit Clock Recovery Cir E4STM1	105	JAWA/JAWG
Jit Clock Recovery Cir STM0	106	JAWA/JAWG
Jit Clock Recovery Cir STM4	107	JAWA/JAWG
Jit Tx Low–Pass Filter	108	JAWA/JAWG
Jit Tx Wander Loop	109	JAWA/JAWG
Jit Tx Jitter Loop	110	JAWA/JAWG
Jitter Generation	111	JAWA/JAWG
Jit Phase Detector	112	JAWA/JAWG
Jit PLL Locking	113	JAWA/JAWG
Jit PLL Gain	114	JAWA/JAWG
Jit Analog Output	115	JAWA/JAWG

GPIB Command. DIAG:SELECT SYSEXTERNAL

Error Messages. See the individual test descriptions for the explanation of possible failures.

Protocol: Misc Register Test

This test verifies the processor's ability to access the Misc Register located on the Main Protocol board.

GPIB Command. DIAG:SELECT:ROUTINE PROTOMISCREG

Notes. This test is destructive to the state of the protocol hardware and therefore re–initializes the Protocol board upon completion.

Error Messages. Potential error messages are as follows:

Test FAIL:

The following error message is produced if the data pattern read back from the hardware differs from the pattern written.

```
Addr: 0x9B0100, Exp: 0xX, Act: 0xX
```

Protocol: SETI Register Test

This test verifies the processor's ability to access the SETI Register located on the High–Speed Protocol board.

GPIB Command. DIAG:SELECT:ROUTINE PROTOSETI

Error Messages. Potential error messages are as follows:

Test FAIL:

The following error message is produced if the data pattern read back from the hardware differs from the pattern written.

```
Addr: 0x9B0C02, Exp: 0xX, Act: 0xX
```

Protocol: Register Access Test

This test verifies the processor's ability to access all of the Protocol board registers. The test provides a quick verification that the board is alive and the various components can be programmed.

The test separates the registers into two categories:

- Read–Only Registers
- Read/Write Registers

The two types of registers are exercised differently. The read–only register exercise does not make any pass/fail decisions based on the contents of the register but simply verifies the register can be read without generating a bus error.

The read/write register exercise is modeled after the standard RAM address–line/data pattern exercise. Each register requires a mask value as not all bits are R/W and some bits affect other registers.

GPIB Command. DIAG:SELECT:ROUTINE PROTOREG

Notes. This test is destructive to the state of the protocol hardware and therefore re–initializes the Protocol board upon completion.

Error Messages. Potential error messages are as follows:

Test FAIL:

The following error message is produced if the read/write portion of the exercise fails. The "Addr" field contains the address of the register that failed.

```
Addr: 0xX, Exp: 0xX, Act: 0xX
```

Protocol: Flash Voltage Test

This test verifies the V_{pp} flash EEPROM programming voltage is disabled.

GPIB Command. DIAG:SELECT:ROUTINE PROTOVFL

Error Messages. Potential error messages are as follows:

Test FAIL:

The following error message indicates the flash EEPROM programming voltage is enabled.

```
Addr: 0x9B0000, Exp: 0x0, Act: 0x1
```

Protocol: Flash Checksum Test

This test verifies the integrity of the protocol board flash EEPROM device using a standard checksum routine.

The checksum routine used is a simple 16–bit summation. The routine reads a 16–bit value from memory and adds it to a running checksum.

GPIB Command. DIAG:SELECT:ROUTINE PROTOCKSUM

Error Messages. Potential error messages are as follows:

Test FAIL:

The following error message is produced if the calculated checksum (“Act”) does not match the value stored in memory (“Exp”).

```
Addr: 0xA8000C, Exp: 0xX, Act: 0xX
```

Protocol: ITX RAM Test

This test verifies the processor interface to the ITX RAM as well as the cell integrity of the memory. The test performs the basic address line/data pattern exercise on both banks of ITX memory.

GPIB Command. DIAG:SELECT:ROUTINE PROTOITX

Notes. The general RAM address line/data pattern routine is slightly modified due to how the memory is accessed. Instead of reading/writing to memory–mapped addresses the routine updates an auto–incrementing set of address counters internal to the ITX FPGA. Also, not all of the data lines are valid and therefore a mask value is required. The data mask for the ITX RAM is: 0x01FF.

Error Messages. For a description of the RAM address line/data line test and possible error messages, refer to *RAM Address/Data Routine* on page -1.

Protocol: IRX RAM Test

This test verifies the processor interface to the IRX RAM as well as the cell integrity of the memory. The test performs the basic address line/data pattern exercise on the entire bank of IRX memory.

GPIB Command. DIAG:SELECT:ROUTINE PROTOIRX

Notes. The general RAM address line/data pattern routine is slightly modified due to how the memory is accessed. Instead of reading/writing to memory–mapped addresses the routine updates an auto–incrementing set of address counters internal to the IRX FPGA. Also, not all of the data lines are valid and therefore a mask value is required. The data mask for the IRX RAM is: 0x00FF.

Error Messages. For a description of the RAM address line/data line test and possible error messages, refer to *RAM Address/Data Routine* on page -1.

Protocol: PRX RAM Test

This test verifies the processor interface to the PRX RAM as well as the cell integrity of the memory. The test performs the basic address line/data pattern exercise on the entire bank of PRX memory.

GPIB Command. DIAG:SELECT:ROUTINE PROTOPRX

Notes. The general RAM address line/data pattern routine is slightly modified due to how the memory is accessed. Instead of reading/writing to memory–mapped addresses the routine updates an auto–incrementing set of address counters internal to the PRX FPGA. Also, not all of the data lines are valid and therefore a mask value is required. The data mask for the PRX RAM is: 0x00FF.

Error Messages. For a description of the RAM address line/data line test and possible error messages, refer to *RAM Address/Data Routine* on page -1.

Protocol: ITX FIFO Test

This test verifies the processor interface to the IRX FIFO RAM as well as the cell integrity of the memory. The routine simply fills the FIFO with an incrementing pattern, then reads out the data and verifies the values are correct.

Note: The CPU is only allowed to write to the FIFO RAM when the incoming data rate is STS–3.

GPIB Command. DIAG:SELECT:ROUTINE PROTOFIFO

Error Messages. Potential error messages are as follows:

Test FAIL - FIFO Active:

The following error message is produced if the FIFO ACT line is asserted after instructing the hardware to halt:

```
FIFO ACTive Stuck High, Exp: 0x0, Act: 0x1
```

Test FAIL - Memory:

The following error message is produced if the data read back from the FIFO does not match the expected value. The “Addr” field indicates which entry in the FIFO contained the failure.

```
Addr: 0xXXXX, Exp: 0xXX, Act: 0xXX
```

Protocol: A/D Converter Test

This test verifies the functionality of the protocol A/D converter. The test verifies that the ADC correctly digitizes the ground and +2.5 V reference signals.

GPIB Command. DIAG:SELECT:ROUTINE PROTOADC

Error Messages. For a description of the verifyADC() routine and possible error messages, refer to *verifyADC(channel, minVal, maxVal) Routine* on page -2.

Protocol: Power Supply Test

This test uses the Power Supply Fault Detect (PSFD) signal on the Protocol board to verify the Protocol board and interface module power supplies.

GPIB Command. DIAG:SELECT:ROUTINE PROTOPS

Error Messages. For a description of the verifyADC() routine and possible error messages, refer to *verifyADC(channel, minVal, maxVal) Routine* on page -2.

Protocol: 52Mb Loop Test

This test verifies the protocol hardware at the 52 MHz data rate. The test uses the serial Tx to Rx loopback path on the Protocol board.

After connecting the internal data path, the routine calls the standard loopback test to exercise the hardware.

GPIB Command. DIAG:SELECT:ROUTINE PROTOLOOP52

Error Messages. For a description of the loopbackTest() routine and possible error messages, refer to *loopbackTest(rate, type) Routine* on page -3.

Protocol: 155Mb Loop Test

This test verifies the protocol hardware at the 155 MHz data rate. The test uses the Tx to Rx loopback path between the SETI and SERI components on the protocol board.

After connecting the internal data path, the routine calls the standard loopback test to exercise the hardware. The exercise is repeated for both electrical (with CMI encoding) and optical (without CMI) paths.

GPIB Command. DIAG:SELECT:ROUTINE PROTOLOOP155

Error Messages. For a description of the loopbackTest() routine and possible error messages, refer to *loopbackTest(rate, type) Routine* on page -3.

Protocol: 622Mb Loop Test

This test verifies the protocol hardware at the 622 MHz data rate. The test uses the Tx to Rx loopback path between the SETI and SERI components on the Protocol board.

After connecting the internal data path, the routine calls the standard loopback test to exercise the hardware.

GPIB Command. DIAG:SELECT:ROUTINE PROTOLOOP622

Error Messages. For a description of the loopbackTest() routine and possible error messages, refer to *loopbackTest(rate, type) Routine* on page -3.

Clock: Internal Reference Test

This test verifies the Clock Generator board's ability to lock on to the internal reference clock.

GPIB Command. DIAG:SELECT:ROUTINE CLKREF

Error Messages. Potential error messages are as follows:

Test FAIL:

```
Phase Lock Failure, Exp: 0x39, Act: 0xXX
```

The above error message is produced if the status of the phase lock loops do not match the expected state (all locked).

Clock: Freq Offset Test

This test verifies the ability of the clock generator board to force frequency offsets into the payload and line clocks.

GPIB Command. DIAG:SELECT:ROUTINE CLKFREQ

Error Messages. Potential error messages are as follows:

Test FAIL - Payload Loss:

The following error message is produced if after railing the payload frequency offset the phase lock loops are not in their expected state. The expected value should indicate that only the internal reference and line offset are locked.

```
Payload PLL Loss Failure, Exp: 0x09, Act:
0xXX
```

Test FAIL - Payload Restore:

The following error message is produced if the phase lock loops do not respond properly when attempting to restore lock on the payload offset.

```
Payload PLL Restore Failure Exp: 0x39, Act:
0xXX
```

Test FAIL - Line Loss:

The following error message is produced if after railing the line frequency offset the phase lock loops are not in their expected state. The expected value should indicate that only the internal reference and both payload offsets are locked.

```
Line PLL Lose Failure, Exp: 0x31, Act: 0xXX
```

Test FAIL - Line Restore:

The following error message is produced if the phase lock loops do not respond properly when attempting to restore lock on the line clock.

```
Line PLL Restore Failure, Exp: 0x39, Act:
0xXX
```

Plug-In Interface Module: Status Test

This test verifies the presence of the Plug–In Interface Module. The Protocol board contains a status bit that indicates whether or not an Plug–In Interface Module is recognized.

GPIB Command. DIAG:SELECT:ROUTINE INTSTAT

Error Messages. Potential error messages are as follows:

Test FAIL:

The following error message indicates the Protocol board did not detect the presence of an Plug–In Interface Module.

```
Addr: 0x9B0000, Exp: 0x0, Act: 0x1
```

Plug-In Interface Module: Identification Test

This test verifies the processor's ability to properly read the Plug–In Interface Module's ID register.

GPIB Command. DIAG:SELECT:ROUTINE INTID

Notes. Before proceeding with the remainder of the test, this routine first verifies that the Plug–In Interface Module is present by performing the O/E Status Test. Refer to *Plug–In Interface Module Status Test*, on page -29, for more information.

Error Messages. Potential error messages are as follows:

Test FAIL:

The following error message is produced if an unknown ID value is reported by the Plug–In Interface Module. The "Act" field contains the ID value read from the hardware.

```
Unknown O/E Module, Exp: 0x7, Act: 0xX
```

Plug-In Interface Module: Access Test

This test verifies the processor's ability to properly access the Plug–In Interface Module for both reading and writing. Communication with the Plug–In Interface Module is done via the I^2C bus. The test uses the Transceiver Control register to perform the access verification.

GPIB Command. DIAG:SELECT:ROUTINE INTACCESS

Notes. Before proceeding with the remainder of the test, this routine first verifies that the Plug–In Interface Module is present by performing the O/E Status Test. Refer to *Plug–In Interface Module Status Test*, on page -29, for more information.

Error Messages. Potential error messages are as follows:

Test FAIL:

The following error message is produced if the data read back from the Plug–In Interface Module is different from the pattern sent. The "Exp" field contains the value written and the "Act" field contains the value read.

```
Addr: 0x72, Exp: 0xX, Act: 0xX
```

Plug-In Interface Module: Tx Optical Power Test

This test verifies the Plug–In Interface Module's optical transmitter by checking the optical power is within a defined tolerance range.

The routine connects the internal Tx to Rx loopback path and verifies the analog signal using the Protocol board A/D converter.

GPIB Command. DIAG:SELECT:ROUTINE INTOPTPWR

Notes. Before proceeding with the remainder of the test, this routine first verifies that the Plug–In Interface Module is present by performing the O/E Status Test. Refer to *Plug–In Interface Module Status Test*, on page -29, for more information.

This test will return PASS without performing the exercise if an electrical–only module is installed.

Error Messages. For a description of the verifyADC() routine and possible error messages, refer to *verifyADC(channel, minVal, maxVal) Routine* on page -2.

Plug-In Interface Module: Rx Signal Level Test

This test verifies the receive signal levels for both optical and electrical inputs. The test requires user interaction to connect external loopback cables to the electrical and optical (if applicable) connectors.

The test uses the A/D converter on the Protocol board to verify the electrical amplitude and optical power of the received signals.

GPIB Command. DIAG:SELECT:ROUTINE INTRXLEV

Notes. Requires user interaction.

Before proceeding with the remainder of the test, this routine first verifies that the Plug–In Interface Module is present by performing the O/E Status Test. Refer to *Plug–In Interface Module Status Test*, on page -29, for more information.

Error Messages. Potential error messages are as follows:

Test FAIL - No Signal:

The following error message is produced if the Plug–In Interface Module does not detect an active input signal. (The ACTIVE SIGNAL status bit is active low.)

```
Active Signal Not Detected, Exp: 0x0, Act:
0x1
```

For a description of the verifyADC() routine and possible error messages, refer to *verifyADC(channel, minVal, maxVal) Routine* on page -2.

Plug-In Interface Module: Internal 52Mb Loop Test

This test verifies the electrical and optical (if applicable) data paths at the 52 MHz rate. The test uses the internal Tx to Rx loopback path.

After connecting the internal data path the routine calls the standard loopback test to exercise the hardware at the specified rate.

GPIB Command. DIAG:SELECT:ROUTINE INTLOOP52I

Error Messages. For a description of the loopbackTest() routine and possible error messages, refer to *loopbackTest(rate, type) Routine* on page -3.

Plug-In Interface Module: Internal 155Mb Loop Test

This test verifies the electrical and optical (if applicable) data paths at the 155 MHz rate. The test uses the internal Tx to Rx loopback path.

After connecting the internal data path the routine calls the standard loopback test to exercise the hardware at the specified rate.

GPIB Command. DIAG:SELECT:ROUTINE INTLOOP155I

Error Messages. For a description of the loopbackTest() routine and possible error messages, refer to *loopbackTest(rate, type) Routine* on page -3.

Plug-In Interface Module: Internal 622Mb Loop Test

This test verifies the optical data path at the 622 MHz rate. The test uses the internal Tx to Rx loopback path.

After connecting the internal data path the routine calls the standard loopback test to exercise the hardware at the specified rate.

GPIB Command. DIAG:SELECT:ROUTINE INTLOOP622I

Notes. This test will return PASS without performing the exercise if an electrical–only module is installed.

Error Messages. For a description of the loopbackTest() routine and possible error messages, refer to *loopbackTest(rate, type) Routine* on page -3.

Plug-In Interface Module: External 52Mb Loop Test

This test verifies the electrical and optical (if applicable) data paths at the 52 MHz rate. The test requires user interaction to connect external loopback cables to the electrical and optical (if applicable) connectors.

This test is identical to the Internal 52Mb Loop except the routine does not connect the internal loopback path. The routine assumes external cabling provides the loopback path.

GPIB Command. DIAG:SELECT:ROUTINE INTLOOP52E

Notes. Requires user interaction.

Error Messages. For a description of the loopbackTest() routine and possible error messages, refer to *loopbackTest(rate, type) Routine* on page -3.

Plug-In Interface Module: External 155Mb Loop Test

This test verifies the electrical and optical (if applicable) data paths at the 155 MHz rate. The test requires user interaction to connect external loopback cables to the electrical and optical (if applicable) connectors.

This test is identical to the Internal 155Mb Loop except the routine does not connect the internal loopback path. The routine assumes external cabling provides the loopback path.

GPIB Command. DIAG:SELECT:ROUTINE INTLOOP155E

Notes. Requires user interaction.

Error Messages. For a description of the loopbackTest() routine and possible error messages, refer to *loopbackTest(rate, type) Routine* on page -3.

Plug-In Interface Module: External 622Mb Loop Test

This test verifies the optical data path at the 622MHz rate. The test requires user interaction to connect external loopback cables to the optical connectors.

This test is identical to the Internal 622Mb Loop except the routine does not connect the internal loopback path. The routine assumes external cabling provides the loopback path.

GPIB Command. DIAG:SELECT:ROUTINE INTLOOP622E

Notes. Requires user interaction.

This test will return PASS without performing the exercise if an electrical–only module is installed.

Error Messages. For a description of the loopbackTest() routine and possible error messages, refer to *loopbackTest(rate, type) Routine* on page -3.

CPU: Vector Interrupt Test

This test verifies the processor's ability to recognize vectored interrupts. The test uses the "TESTVECTINT" bit in the Processor board Control Register to force the interrupt.

The Multi–Function Peripheral (MFP) chip is programmed to recognize the interrupt on the rising edge. The interrupt is then unmasked and enabled.

Before exiting, the interrupt is disabled and masked.

GPIB Command. DIAG:SELECT:ROUTINE CPUINT

Error Messages. Potential error messages are as follows:

Test FAIL - Unexpected Interrupt:

```
Interrupt Count Exp: 0x0, Act: 0xX
```

This message is produced if an interrupt is detected prior to forcing the interrupt. The "Act" value indicates the number of times the interrupt occurred.

Test FAIL - No Interrupt:

```
Interrupt Count Exp: 0x1, Act: 0xX
```

This message is produced if an incorrect number of interrupts occurred after forcing a single interrupt. The "Act" value indicates the number of interrupts that occurred. Typically if the test fails with this message the "Act" value will be 0, meaning the routine expected an interrupt but did not detect one.

CPU: IIC Control Test

This test verifies the processor's ability to access the I^2C–bus controller chip. The test performs a write/read verification on the data register of the controller IC.

The test first polls the busy bit in the status register of the I^2C–bus controller chip to wait until the controller is not busy. If after a defined number of attempts the chip is still busy, the test will give up and fail.

GPIB Command. DIAG:SELECT:ROUTINE CPUIIC

Error Messages. Potential error messages are as follows:

Test FAIL - IIC Busy:

```
Addr: 0x4000000, Exp: 0x1, Act: 0x0
```

This error message is produced if the I^2C controller remains busy while the test is attempting to access the chip.

Test FAIL - IIC Access:

```
Addr: 0x4000000, Exp: 0xXX, Act: 0xXX
```

This error message is produced if the test was unsuccessful in its attempt to modify the contents of the data register.

CPU: Clock/Calendar Test

This test verifies the functionality of the clock/calendar IC. If the test is invoked as part of the Self Test suite, the routine simply performs an access verification. Otherwise, the test also verifies the chip's 1 second interrupt.

All communication with the clock/calendar chip is via the I^2C controller chip. The test issues a set NODA (NO DAte) command and verifies the flag is set. Then the test repeats the exercise by clearing the NODA flag.

If the exercise passes and the test was not invoked as part of the Self–Test suite (which includes power–up self–test) additional verifications of the chip's ability to keep time are performed.

The test first monitors the second output to verify it is changing state. The second output should change state every 0.5 seconds. If this exercise passes the test then it verifies the 1 second interrupt. The delay loops used in the routines should be roughly 5 seconds. The tests do not verify the accuracy of the second pulse, but whether or not it is changing at all.

The routine for verifying the second interrupt is similar to the exercise described above, except the routine monitors the value of a software variable that gets updated each time the second interrupt occurs. If the variable does not change within 5 seconds the test fails (Test FAIL - Second Interrupt).

GPIB Command. DIAG:SELECT:ROUTINE CPUCLKCAL

Notes. The clock/calendar chip is an I^2C-bus component. Therefore, this test depends on the functionality of the I^2C-bus controller and circuitry.

Error Messages. Potential error messages are as follows:

Test FAIL - Set NODA:

```
Addr: 0xD0, Exp: 0x1, Act: 0x0
```

This error message is produced if the instrument was unsuccessful in its attempt to set the NODA flag within the clock/calendar chip.

Test FAIL - Reset NODA:

```
Addr: 0xD0, Exp: 0x0, Act: 0x1
```

This error message is produced if the instrument was unsuccessful in its attempt to clear the NODA flag after it was previously set.

Test FAIL - Timing:

```
Addr: 0xD0, Exp: 0x0/0x1, Act: 0x1/0x0
```

This error message is produced if the second output did not change state after monitoring for 5 seconds. The "Exp" value will either be 0 or 1 and the "Act" value will then be the opposite value.

Test FAIL - Second Interrupt:

```
Seconds Count, Exp: 0xXX, Act: 0xXX
```

This error message is produced if the second interrupt failed to occur after a 5 second delay.

CPU: Clk/Cal Battery Test

This routine verifies the +3V battery used to power the clock/calendar IC during the instrument down time. The clock/calendar chip contains a Power Fail flag that is set if the external battery drops below the threshold value.

This test simply examines the state of the Power Fail flag in the clock/calendar chip.

GPIB Command. DIAG:SELECT:ROUTINE CPUCCBATT

Notes. The clock/calendar chip is an I^2C bus component and therefore dependent on the functionality of the I^2C bus controller IC and circuitry.

Once the power fail bit is set, the flag will remain set (even after the battery is restored) until the chip is reprogrammed.

Error Messages. Potential error messages are as follows:

Test Fail:

```
Addr: 0xD0, Exp: 0x0, Act: 0x1
```

The above error message indicates the power fail flag is set.

CPU: DUART Test

This test verifies the DUART chip. If the test is invoked as part of the Self Test suite the routine simply performs an access verification. Otherwise more thorough testing of the chip data paths and interrupts are done.

The routine is the access verification portion of the test. The test uses the Interrupt Vector Register to perform the exercise.

If the exercise passes and the test was not invoked as part of the Self–Test suite (which includes power–up self–test) additional testing is performed. These additional exercises are repeated on both channels of the DUART. If a failure is detected, the test will abort (that is, no further testing is done) and report the error.

The first extended test is the interrupt verification. The test exercises the chip in local loopback mode and verifies the Tx interrupt. The interrupt handler for the Tx interrupt places the “txData” in the transmit register then shifts “txData” left by 1. Knowing this, the test routine sets “txData” to 0x80, enables the Tx interrupt, and performs a small delay. The routine then verifies the “txData” was shifted to 0x00 by the interrupt handler.

The final extended exercise is the loopback test. This exercise verifies the DUART’s ability to transmit and receive data under interrupt control. Again, the DUART is placed in local loopback mode. The interrupt handler is responsible for the following tasks:

- Tx Side: Place “txData” in transmit register and shift “txData” left by 1. Disable Tx interrupt if “txData” is 0.
- Rx Side: Read receive register and place data in “rxData[]” array. Disable Rx interrupt if “rxData[]” is full.

GPIB Command. DIAG:SELECT:ROUTINE CPUDUART

Error Messages. Potential error messages are as follows:

Test FAIL - Access:

```
Addr: 0x500000C, Exp: 0xAA/0x55, Act: 0xXX
```

The above error message is produced if the test was unsuccessful in its attempts to access the DUART Interrupt Vector Register. The “Exp” value will either be 0xAA or 0x55.

Test FAIL - Interrupt:

```
Addr: 0x5000005, Exp: 0x1/0x10, Act: 0x0
```

The above error message is produced if the Tx interrupt failed to occur. The “Exp” value will be 0x1 for channel A and 0x10 for channel B.

Test FAIL - Loopback:

```
Addr: 0x500000F/0x500002F, Exp: 0xXX, Act:
0xXX
```

The above error message is produced if the loopback exercise failed. The “Addr” value will be 0x500000F for channel A and 0x500002F for channel B.

Display: Video RAM Test

This test verifies the display board video RAM. The test performs both a data–line– and an address–line/data pattern exercise on each of the bit–planes.

If this test is invoked as part of the self–test suite (which includes power–up self–test) the routine will use an abbreviated list of test patterns.

Each bit–plane is 1024x512 pixels (or 64 Kbytes). The graphics bit–plane uses this entire area, while the user interface planes only use the first 480 rows (or 60 Kbytes). The memory tests exercise only the portion of memory which is actually used.

GPIB Command. DIAG:SELECT:ROUTINE DISPRAM

Error Messages. For a description of the RAM Data Line Routine and possible error messages, refer to *RAM Data Line Routine* on page -1.

For a description of the RAM address line/data line test and possible error messages, refer to *RAM Address/Data Routine* on page -1.

Display: RAMDAC Test

This test verifies the color palette memory of the RAM DAC. The test performs a simple data pattern exercise.

GPIB Command. DIAG:SELECT:ROUTINE DISPDAC

Error Messages. Potential error messages are as follows:

Test FAIL:

```
Addr: 0x990001, Exp: 0xXX, Act: 0xXX
```

Display: White Field Test

This test fills the screen with a solid high-intensity pattern. The test requires user interaction to verify the screen is filled with a uniform intensity.

This test programs the RAM DAC to produce 100% intensity output, then updates the appropriate video bit–plane with a solid filled box.

GPIB Command. DIAG:SELECT:ROUTINE DISPWF

Notes. Requires user interaction.

Error Messages. None.

Display: Grey Field Test

This test fills the screen with a solid medium–intensity pattern. The test requires user interaction to verify the screen is filled with a uniform intensity of the appropriate level.

This test programs the RAM DAC to produce 30% intensity output, then updates the appropriate video bit–plane with a solid filled box.

GPIB Command. DIAG:SELECT:ROUTINE DISPGF

Notes. Requires user interaction.

Error Messages. None.

Display: White Box Test

This test draws two solid boxes, one high-intensity box centered within a longer medium intensity box. The test is useful for visually comparing the contrast in intensity levels.

GPIB Command. DIAG:SELECT:ROUTINE DISPWB

Notes. Requires user interaction.

Error Messages. None.

Display: Test Grid Test

This test draws a test grid on the screen. The test is useful for determining if the display is properly centered.

GPIB Command. DIAG:SELECT:ROUTINE DISPTG

Notes. Requires user interaction.

Error Messages. None.

Display: Composite Test

This test draws a test grid along with various line-filled boxes of differing orientation. The test is useful for identifying geometric distortions in the CRT.

GPIB Command. DIAG:SELECT:ROUTINE DISPCOMP

Notes. Requires user interaction.

Error Messages. None.

Display: HW Scrolling Test

This test exercises the hardware scrolling machinery. The test requires user interaction to verify that the scrolling checkerboard pattern scans completely and smoothly (no jumps) in both the horizontal and vertical direction.

GPIB Command. DIAG:SELECT:ROUTINE DISPSCROLL

Notes. Requires user interaction.

Error Messages. None.

Front Panel General Notes

The processor communicates with the front panel using the A Channel of the MC68681 DUART (located on the processor board). All diagnostics are done with the interrupts disabled. The software polls the hardware to determine the status of the transmitter/receiver when sending/receiving bytes. This polling method has an associated timeout. If the hardware does not respond within the allotted time, the test fails and produces one of the error messages described in the following *Front Panel Error Messages* section.

In transitioning from an interrupt–driven to a polling method of controlling the communication hardware, the routine needs to send a dummy command to the Front Panel after disabling the interrupts. This dummy command is performed as the first step in all of the Front Panel tests. The op–code of this NOP command is:

Front Panel NOP Command: 0xC0

When the instrument is first powered on, the host processor and the front panel processor perform an initialization sequence to properly recognize and configure the hardware. During this hardware initialization phase if a failure is detected the Self–Test diagnostics will report one of the error messages described in the following *Front Panel Error Messages* section.

Front Panel Error Messages

Test FAIL - Sending Bytes To Front Panel:

```
Time-Out Sending All Bytes, Exp: 0xXX, Act:
0xXX
```

This error message is produced if the front panel is not ready to receive the next byte of a command within a reasonable amount of time. The “Exp” value contains the number of bytes in the command the software was attempting to send. The “Act” value contains the actual number of bytes successfully sent.

Test FAIL - Receiving Bytes From Front Panel:

```
Time-Out Reading All Bytes, Exp: 0xXX, Act:
0xXX
```

This error message is produced if the DUART does not receive the next byte of a response from the front panel within a reasonable amount of time. The “Exp”

value contains the number of bytes in the response the software was expecting to receive. The “Act” value contains the actual number of bytes successfully read.

Test FAIL - Self–Test Status:

```
Front Panel Status Byte, Exp: 0xE0, Act: 0xXX
```

The first byte after power–up reported by the front panel processor is the status of its internal self–test. The “Exp” field contains the expected status while the “Act” field contains the actual results.

Test FAIL - Self–Test Communication:

```
Front Panel Data Byte, Exp: 0xXX, Act: 0xXX
```

If the front panel passes its internal self–test, the two processors will then attempt to verify the communication path by having the host processor send the following sequence of bytes to the front panel which simply echoes the characters back:

```
0xA5, 0x4B, 0x96, 0x2D
```

The error message shown above is produced if the bytes received do not match the bytes sent.

Front Panel: Internal Test

This test instructs the front panel processor to perform its internal self–test and report back the results.

GPIB Command. DIAG:SELECT:ROUTINE FPINT

Notes. Refer to *Front Panel General Notes* on page -41 for a description of other possible failure modes relating to front panel communication.

Error Messages. Potential error messages are as follows:

Test FAIL:

```
Status Byte Contains Error, Exp: 0xE0, Act:
0xXX
```

The “Exp” field contains the expected status for No Failures, while the “Act” field contains the actual self–test status reported by the front panel processor.

Front Panel: LEDs Test

This test exercises each of the front panel LEDs. Although the front panel processor contains a LED test that can be invoked on demand, the order in which the LEDs are lighted is hard to follow. Therefore, the LEDs are explicitly controlled by the host processor.

This test requires user interaction to verify the LEDs light in the correct order and that only one LED is lighted at a time. Skipping over LEDs or lighting multiple LEDs simultaneously would be considered a failure.

The test exercises the set of front panel LEDs in the following order:

YELLOW LEDs (Starting at top of the left column)

RED LEDs (Starting at top of the left column)

GREEN LEDs (Starting with status LEDs, then lighting top row of functions LEDs right to left)

This test uses two separate front panel LED commands. The first form turns on/off a single LED. The second form requires two LED IDs, and turns the first LED off and the second one on.

GPIB Command. DIAG:SELECT:ROUTINE FPLEDS

Notes. Requires user interaction.

Refer to *Front Panel General Notes* on page -41 for a description of other possible failure modes relating to front panel communication.

Error Messages. None.

Front Panel: Speaker Test

This test instructs the front panel to "ring" the bell. The test requires user interaction to verify the bell does indeed make the appropriate sound.

GPIB Command. DIAG:SELECT:ROUTINE FPSPKR

Notes. Requires user interaction.

Refer to *Front Panel General Notes* on page -41 for a description of other possible failure modes relating to front panel communication.

Error Messages. None.

Front Panel: Manual Test

This test provides an interactive verification of the front panel buttons and knob. The test requires user interaction and provides visual feedback of button presses and knob turns.

GPIB Command. DIAG:SELECT:ROUTINE FPINTR

Notes. Requires user interaction.

Refer to *Front Panel General Notes* on page -41 for a description of other possible failure modes relating to front panel communication.

Error Messages. None.

Disk: PM110 Register Test

This test verifies the processor's ability to access the internal registers of the PM110 ASIC by performing a walking 1's exercise on various registers.

GPIB Command. DIAG:SELECT:ROUTINE DISKREG

Error Messages. For a description of the RAM Data Line Routine and possible error messages, refer to *RAM Data Line Routine* on page -1.

The RAM Data Line exercise performed is for byte wide memory.

Disk: PM110 Cache Test

This test verifies the integrity of the PM110 cache memory by performing an address line/data pattern exercise on the entire memory range.

GPIB Command. DIAG:SELECT:ROUTINE DISKCACHE

Error Messages. For a description of the RAM address line/data line test and possible error messages, refer to *RAM Address/Data Routine* on page -1.

The RAM Address Line/Data Pattern exercise is for byte–wide memory.

Disk: PM110 Counter Test

This test verifies the internal counters of the DMA portion of the PM110. The exercise manually increments the counters and verifies the terminal count status responds at the correct location.

GPIB Command. DIAG:SELECT:ROUTINE DISKCNTR

Error Messages. Test FAIL - Terminate Early:

The following error message is produced if the terminal count status is high before the counter reaches the end count. The "Act" field contains the count value when the status went high.

```
Addr: 0x980001, Exp: 0x0, Act: 0xX
```

Test FAIL - No Termination:

The following error message is produced if the terminal count status fails to go high after the counter expires.

```
Addr: 0x980001, Exp: 0x0, Act: 0x0
```

Disk: Controller Test

This test initializes the DP8473 Floppy Disk Controller and verifies “No Errors” were reported.

GPIB Command. DIAG:SELECT:ROUTINE DISKCONT

Error Messages. Potential error messages are as follows:

Test Fail:

```
Unable to Initialize dp8473, Exp: 0x1, Act:
0x0
```

Disk: Disk Drive Test

The above error message indicates the routine used to initialize the Floppy Disk Controller returned with an error status.

This test verifies the floppy disk drive responds properly when initialized.

GPIB Command. DIAG:SELECT:ROUTINE DISKDRV

Notes. Since the floppy drive plastic bezel can warp if subjected to the cycle room, the floppy is not installed during cycle room testing. The test reads protocol board DIP switch 3 as an indicator the drive is not installed. If the switch is set, the test simply returns PASSED without attempting to access the missing hardware.

Error Messages. Potential error messages are as follows:

Test FAIL - Disk Controller:

```
dp8473 not initialized, Exp: 0x1, Act: 0x0
```

The above error message indicates the routine used to initialize the Floppy Disk Controller returned with an error status.

Test FAIL - Disk Drive:

```
Unable to Init Floppy Drive, Exp: 0x1, Act:
0x0
```

The above error message indicates the routine used to initialize the Floppy Drive returned with an error status.

Disk: Format & Verify Test

This test verifies the ability to properly format and label a disk. The test requires user interaction to insert a disk in the drive before invoking the test.

GPIB Command. DIAG:SELECT:ROUTINE DISKFNV

Notes. Requires user interaction.

This test erases the contents of the disk.

Error Messages. Potential error messages are as follows:

Test FAIL - File Open:

The following error message is produced if the test fails to gain access to the disk for performing disk operations.

```
Unable to open " fd0:/" , Exp: 0x1, Act: 0x0
```

Test FAIL - Format:

The following error message is produced if the disk FORMAT operation reports an error status.

```
Unable to format floppy disk, Exp: 0x1, Act:
0x0
```

Test FAIL - Init:

The following error message is produced if the disk INITIALIZE operation reports an error status.

```
Unable to init floppy disk, Exp: 0x1, Act:
0x0
```

Test FAIL - Label:

The following error message is produced if the disk LABEL operation reports an error status.

```
Unable to Label floppy disk, Exp: 0x1, Act:
0x0
```

Test FAIL - File Close:

The following error message is produced if the test fails to close the file upon completion of the test.

```
Unable to close floppy disk, Exp: 0x1, Act:
0x0
```

Disk: Dysan Seek Test

This test requires a special Dysan disk (DDD 305-400 P/N 810244) to perform the exercise. The test reads selected tracks using both heads to check for a specified pattern on the disk. If any of the tracks fail, the test fails.

The test requires user interaction to insert the Dysan disk into the drive prior to invoking the test.

GPIB Command. DIAG:SELECT:ROUTINE DISKSEEK

Notes. Requires user interaction.

Error Messages. Potential error messages are as follows:

Test FAIL - Disk Drive:

The following error message indicates the routine used to initialize the Floppy Drive returned with an error status.

```
Floppy Drive Not Initialized, Exp: 0x1, Act:
0x0
```

Test FAIL - Disk Read:

The following error message is produced if the test fails when attempting to read the Dysan ID string.

```
Unable to Read Dysan Disk, Exp: 0x1, Act: 0x0
```

Test FAIL - Dysan ID:

The following error message is produced if the Dysan ID string read from the disk is not as expected.

```
Incorrect ID for Dysan Disk, Exp: 0x1, Act:
0x0
```

Test FAIL - Sector Read:

Once inside the test loop of examining specific locations on the disk, the following error message will be produced if the test reads an unexpected number of bytes from the disk.

```
Incorrect number of bytes read from disk,
          Exp: 0x1, Act: 0x0
```

Test FAIL - Sector ID:

Once inside the test loop of examining specific locations on the disk, the following error message will be produced if the test reads an incorrect ID string from the disk.

```
Incorrect id read from disk, Exp: 0x1, Act:
0x0
```

Tributary General Notes

This section describes tests you can use to troubleshoot the tributary circuitry, For each test, this section gives a brief description of the test, its GPIB command, and possible error messages.

Tributary Trib Flash Voltage Test

This test checks for the flash ROM program voltage enabled.

The voltage level of the program voltage is read through the status register and indicates when +12 V is applied to the flash ROM.

GPIB Command. DIAG:SELECT:ROUTINE TRIBVFL

Notes. Accessed by initiating the complete tributary diagnostics.

Error Messages. Potential error messages are as follows:

Test FAIL:

```
" Tributary Flash VPP Voltage is ON"
```

Tributary Trib Flash Checksum Test

This test verifies the integrity of the tributary board flash EEPROM device using a standard checksum routine.

The checksum routine used is a simple 16–bit summation. The routine reads a 16–bit value from memory and adds it to a running checksum.

GPIB Command. DIAG:SELECT:ROUTINE TRIBCKSUM

Notes. Accessed by initiating the complete tributary diagnostics.

Error Messages. Potential error messages are as follows:

Test FAIL:

The following error message is produced if the calculated checksum ("Act") does not match the value stored in memory ("Exp").

```
Addr: 0xA8000C, Exp: 0xX, Act: 0xX
```

Tributary: DSn Test Set

This test verifies the ability of the tributary hardware to generate and receive DSn alarms, errors, framing formats, and patterns. This is accomplished by looping the test set transmitter to its receiver. Both the mapper/demapper and line interface are disconnected during this test.

These tests are the basic building blocks of all tributary diagnostics. Therefore, if these tests fail then the rest of the tributary diagnostics will also fail.

This routine calls the standard DSn test set tests to exercise the hardware.

GPIB Command. DIAG:SELECT:ROUTINE TRIBDS1TS
DIAG:SELECT:ROUTINE TRIBDS3TS

Notes. None.

Error Messages. See *diagGroupTestSet (Tributary Rate)*, on page -5, for a list of possible error messages.

Tributary: En Test Set

This test verifies the ability of the tributary hardware to generate and receive En alarms, errors, framing formats, and patterns. This is accomplished by looping the test set transmitter to its receiver. Both the mapper/demapper and line interface are disconnected during this test.

These tests are the basic building blocks of all tributary diagnostics. Therefore, if these tests fail then the rest of the tributary diagnostics will also fail.

This routine calls the standard En test set tests to exercise the hardware.

GPIB Command. DIAG:SELECT:ROUTINE TRIBE1TS
DIAG:SELECT:ROUTINE TRIBE3TS

Notes. None.

Error Messages. See diagGroupTestSet (Tributary Rate), on page -5, for a list of possible error messages.

Tributary: Register Access

This test verifies the ability of the processor to access all tributary board registers. The test provides a quick verification that the board is alive and that various components can be programmed.

The test is modeled after the standard RAM address–line/data pattern routine. Each register requires a mask value as not all bits are R/W and some bits affect other registers.

GPIB Command. DIAG:SELECT:ROUTINE TRIBREG

Notes. This test is destructive to the state of the tributary hardware and therefore re-initializes the Tributary board upon completion.

Error Messages. Potential error messages are as follows:

Test FAIL:

The following error message is produced if the read/write portion of the routine fails. The “Addr” field contains the address of the register that failed.

```
Addr: 0xX, Exp: 0xX, Act: 0xX
```

Tributary: DSn Line Interface (External Loopback)

This test verifies the tributary hardware between the test set and line interface. This is accomplished by connecting the test set to the line interface through the configuration switch. The mapper/demapper is disconnected during this test.

The test uses the Tx to Rx external loopback path at the DSn line interface. An external cable is required at the DSn connectors to run this test.

This routine calls the standard DSn line interface loopback test to test the hardware.

GPIB Command. DIAG:SELECT:ROUTINE TRIBDS1LIFE
DIAG:SELECT:ROUTINE TRIBDS3LIFE

Notes. None.

Error Messages. See *diagGroupLineInterface(Tributary Rate, Loopback)*, on page -8, for a list of possible error messages.

Tributary: En Line Interface (External Loopback)

This test verifies the tributary hardware between the test set and line interface. This is accomplished by connecting the test set to the line interface through the configuration switch. The mapper/demapper is disconnected during this test.

The test uses the Tx to Rx external loopback path at the En line interface. An external cable is required at the En connectors to run this test.

GPIB Command. DIAG:SELECT:ROUTINE TRIBE1LIFE
DIAG:SELECT:ROUTINE TRIBE3LIFE
DIAG:SELECT:ROUTINE TRIBE4LIFE
DIAG:SELECT:ROUTINE TRIBM45LIFE

Notes. None.

Error Messages. See *diagGroupLineInterface(Tributary Rate, Loopback)*, on page -8, for a list of possible error messages.

Tributary: DSn Line Interface (Internal Loopback)

This test verifies the tributary hardware between the test set and line interface. This is accomplished by connecting the test set to the line interface through the configuration switch. The mapper/demapper is disconnected during this test.

The test uses the Tx to Rx loopback path at the DSn line interface. An external cable is not required at the DSn connectors to run this test.

This routine calls the standard DSn line interface loopback test to test the hardware.

GPIB Command. DIAG:SELECT:ROUTINE TRIBDS1LIFI
DIAG:SELECT:ROUTINE TRIBDS3LIFI

Notes. None.

Error Messages. See *diagGroupLineInterface(Tributary Rate, Loopback)*, on page -8, for a list of possible error messages.

Tributary: En Line Interface (Internal Loopback)

This test verifies the tributary hardware between the test set and line interface. This is accomplished by connecting the test set to the line interface through the configuration switch. The mapper/demapper is disconnected during this test.

The test uses the Tx to Rx loopback path at the En line interface. An external cable is not required at the En connectors to run this test.

This routine calls the standard En line interface loopback test to test the hardware.

GPIB Command. DIAG:SELECT:ROUTINE TRIBE1LIFI
DIAG:SELECT:ROUTINE TRIBE3LIFI
DIAG:SELECT:ROUTINE TRIBE4LIFI

Notes. None.

Error Messages. See *diagGroupLineInterface(Tributary Rate, Loopback)*, on page -8, for a list of possible error messages.

Tributary: DSn Mapper/Demapper

This test verifies the ability of the tributary hardware to generate and receive VT failures, alarms, errors, background patterns, and background framing formats. This is accomplished by connecting the test set to the mapper/demapper through the configuration switch. The line interface is disconnected during this test.

This routine calls the standard DSn mapper/demapper tests.

GPIB Command. DIAG:SELECT:ROUTINE TRIBVTMAP
DIAG:SELECT:ROUTINE TRIBDS3MAP

Notes. None.

Error Messages. See the *diagGroupMapDemap (Tributary Rate)*, on page -9, for a list of possible error messages.

Tributary: En Mapper/Demapper

This test verifies the ability of the tributary hardware to generate and receive TU failures, alarms, errors, background patterns, and background framing formats. This is accomplished by connecting the test set to the mapper/demapper through the configuration switch. The line interface is disconnected during this test.

This routine calls the standard En mapper/demapper tests.

GPIB Command. DIAG:SELECT:ROUTINE TRIBTU12MAP
DIAG:SELECT:ROUTINE TRIBTU3MAP
DIAG:SELECT:ROUTINE TRIBE4MAP
DIAG:SELECT:ROUTINE TRIBM45MAP

Notes. None.

Error Messages. See the *diagGroupMapDemap (Tributary Rate)*, on page -9, for a list of possible error messages.

Tributary: DSn Ring

This test verifies the overall operation of the Tributary board by connecting all the major tributary hardware blocks (test set, mapper/demapper, and line interface) through the configuration switch. Once all the blocks are connected, various VT and DSn alarms, errors, and failures are tested.

Ring Configuration: (Test Set (Tx) -> (Rx) Mapper/Demapper (Tx)
-> (Rx) Line Interface (Tx) -> (Rx) Test Set)

This test should be run after all the other tributary tests have passed.

This routine calls the standard DSn ring test.

GPIB Command. DIAG:SELECT:ROUTINE TRIBDS1RING
DIAG:SELECT:ROUTINE TRIBDS3RING

Notes. None.

Error Messages. See the *diagTribRing(Tributary Rate)*, on page -12, for a list of possible error messages.

Tributary: En Ring

This test verifies the overall operation of the Tributary board by connecting all the major tributary hardware blocks (test set, mapper/demapper, and line interface) through the configuration switch. Once all the blocks are connected, various TU and En alarms, errors, and failures are tested.

Ring Configuration: (Test Set (Tx) -> (Rx) Mapper/Demapper (Tx)
-> (Rx) Line Interface (Tx) -> (Rx) Test Set)

This test should be run after all the other tributary tests pass.

This routine calls the standard En ring test.

GPIB Command. DIAG:SELECT:ROUTINE TRIBE1RING
DIAG:SELECT:ROUTINE TRIBE3RING
DIAG:SELECT:ROUTINE TRIBM45RING

Notes. None.

Error Messages. See the *diagTribRing(Tributary Rate)*, for a list of possible error messages.

Jitter/Wander General Notes

This section describes tests you can use to troubleshoot the jitter/wander generation and measurement circuitry, For each test, this section gives a brief description of the test, its GPIB command, and possible error messages.

Jawa: Clock Recover Circuit

This test verifies the operation of the JAWA clock recovery circuit. There is a separate test for each rate. The 155 Mb/s test also tests the 140 Mb/s rate.

GPIB Commands. DIAG:SELECT:ROUTINE JMEACR2M
DIAG:SELECT:ROUTINE JMEACR34M
DIAG:SELECT:ROUTINE JMEACR155M
DIAG:SELECT:ROUTINE JMEACR52M
DIAG:SELECT:ROUTINE JMEACR622M

Error Messages. Potential error messages are as follows:

Test FAIL:

The following error message is produced if the clock recovery circuit cannot be disabled (in this error message, the data xxx is meaningless):

```
CRC undisable, Exp: xxx, Act: xxx
```

The following error message is produced if the clock recovery circuit cannot be enabled (in this error message, the data xxx is meaningless):

```
CRC unenable, Exp: xxx, Act: xxx
```

The following error message is produced if the oscillator will not tune over the proper frequency range:

<data rate>, Exp: <limit frequency>, Act: <measured frequency>

The following error message is produced if the oscillator will not synchronize:

<data rate>, Exp: <expected frequency>, Act: <measured frequency>

Jawa: Register Access

This test verifies the registers on the JAWA and JAWG boards.

GPIB Command. DIAG:SELECT:ROUTINE JITREG

Error Messages. Potential error messages are as follows:

Test FAIL:

The following error message is produced if the read/write portion of the test fails:

> Addr: <register address>, Exp: <value written>, Act: <value read>

Jawa: Flash Memory Checksum

This test verifies the JAWA EEPROM using a checksum algorithm.

GPIB Command. DIAG:SELECT:ROUTINE JMEACKSUM

Error Messages. Potential error messages are as follows:

Test FAIL:

The following error message is produced if the proper flash memory header is not read:

> Addr: <start address of flash>, Exp: 0xc3a5, Act: <ID read>

The following error message is produced if the calculated checksum does not match the value stored in memory:

> Addr: <start address of checksum>, Exp: <calculated>, Act: <read from flash>

Jawa: DAC Loopback

This test verifies the multiple–output DAC on the JAWA board.

GPIB Command. DIAG:SELECT:ROUTINE JITDACLB

Error Messages. Potential error messages are as follows:

Test FAIL:

The following error message is produced if the read value does not match the written value to within a specific tolerance:

> Addr: 0xb1a018, Exp: <value written>, Act: <value read>

Jawa: Clock Recovery Divider

This test verifies the function of the clock recovery divider.

GPIB Command. DIAG:SELECT:ROUTINE JMEADIVA

Error Messages. Potential error messages are as follows:

Test FAIL:

The following error message is produced if two computed frequencies do not match:

> `freq diff<100kHz, Exp: 0x186a0, Act:` <difference between computed frequencies>

Jawa: Tracking PLL

This test verifies the function of the tracking phase locked loop.

GPIB Command. DIAG:SELECT:ROUTINE JMEATRL

Error Messages. Potential error messages are as follows:

Test FAIL:

The following error message is produced if the loop fails to lock:

> `freq diff<thresh, Exp: 0x186a0, Act:` <measured frequency difference>

The following error message is produced if the loop fails to unlock when it should:

> `can't unlock, Exp:` <frequency limit (max)>`, Act:` <measured frequency>

Jawa: Measurement Phase Detector

This test verifies the function of the phase detector in the measurement phase locked loop.

GPIB Command. DIAG:SELECT:ROUTINE JMEAMPLPHDET

Error Messages. Potential error messages are as follows:

Test FAIL:

The following error message is produced if the loop amplitude is correct (reference amplitude is measured with 1.3 MHz filter):

> `Minimum:` <40% of reference amplitude>`, Maximum:` <60% of reference amplitude>`, Actual:` <measured value with 400 kHz filter>

Jawa: Measurement PLL Locking

This test verifies the function of the measurement phase locked loop.

GPIB Command. DIAG:SELECT:ROUTINE JMEAMPLOCK

Error Messages. Potential error messages are as follows:

Test FAIL:

The following error message is produced if the loop does not lock:

```
PLL can't lock, Exp: 0x0, Act: 0x1
```

Jawa: Measurement PLL Gain

This test verifies the function of the measurement phase locked loop.

GPIB Command. DIAG:SELECT:ROUTINE JMEAMPGAIN

Error Messages. Potential error messages are as follows:

Test FAIL:

The following error message is produced if the loop does not lock:

`VGA Fail@STM1E, Exp: 0x2, Act:` <measured gain ratio>

Jawa: FIFO

This test verifies that the FIFO can be written and read.

GPIB Command. DIAG:SELECT:ROUTINE JMEAFIFO

Error Messages. Potential error messages are as follows:

Test FAIL:

The following error message is produced if the FIFO reports full immediately after being reset:

```
FIFO Active Stuck High, Exp: 0x0, Act: 0x1
```

The following error message is produced if the value written to the FIFO does not match the value read back from it:

`Addr:` <offset in FIFO of difference>`, Exp:` <value written>`, Act:` <value read>

Jawa: Analog Output

This test verifies that the path between jitter generation and jitter measurement is working.

GPIB Command. DIAG:SELECT:ROUTINE JMEAAOUT

Error Messages. Potential error messages are as follows:

Test FAIL:

The following error message is produced if the analog output calibration fails:

```
A out cal failed, Exp: 0x0, Act: 0x0
```

The following error message is produced if the proper frequency is not measured at the analog output:

<data rate>, Exp: <expected frequency>, Act: <measured frequency>

Jawa: Wander Loop Locking

This test verifies phase locked loop that is used to generate wander. The test checks that the loop is initially locked, that it will unlock on command, and reacquire a lock on command.

GPIB Command. DIAG:SELECT:ROUTINE JGENWLLOCK

Error Messages. Potential error messages are as follows:

The following error message is produced if the PLL will not lock:

wander loop unlock, Exp: 0x63, Act: <measured frequency difference>

The following error message is produced if the PLL will not unlock:

wander loop not unlock, Exp: <VCO frequency limit>, Act: <measured frequency difference>

Jawa: Jitter Loop Locking

This test verifies phase locked loop that is used to generate jitter. The test checks that the loop locks for all rates and ranges and that the loop is not oscillating.

GPIB Command. DIAG:SELECT:ROUTINE JGENJLLOCK

Error Messages. Potential error messages are as follows:

Test FAIL:

The following error message is produced if the offset calibration fails:

<data rate> <range> `UI cal fail, Exp: 0x1, Act: 0x0`

The following error message is produced if the loop does not lock:

<data rate> <range> `UI lock fail, Exp: 0x1, Act: 0x0`

Jawa: Jitter Loop Low-Pass Filters

This test verifies the selectable low–pass filters in the jitter generator phase locked loop.

GPIB Command. DIAG:SELECT:ROUTINE JGENJLPF

Error Messages. Potential error messages are as follows:

Test FAIL:

The following error message is produced if the offset calibration fails:

<filter bandwidth> `cal fail, Exp: 0x1, Act: 0x0`

The following error message is produced if the loop does not lock:

<filter bandwidth> `lock fail, Exp: 0x1, Act: 0x0`

Jawa: Jitter Generation

This test verifies that the JAWG hardware is producing jitter.

GPIB Command. DIAG:SELECT:ROUTINE JGENFUNC

Error Messages. Potential error messages are as follows:

Test FAIL:

The following error message is produced if the offset calibration fails:

`JGEN loop offset won’t cal, Exp: 0x1, Act: 0x0`

The following error message is produced if the loop does not lock:

```
JGEN loop unlock@STM1E, Exp: 0x1, Act: 0x0
```

The following error message is produced if the peak amplitude reading is too low to indicate jitter:

```
peak det low@STM1E, Exp: 0x1f4, Act: <peak reading>
```

Notes. The test does not rely on the jitter measurement hardware.

Troubleshooting Sequence

The Troubleshooting Sequence allows qualified technicians to determine which board in a CTS instrument to replace. You use the results of the CTS Diagnostics to make this determination. The troubleshooting sequence assumes that you are familiar with the CTS Diagnostic System and its use.

The troubleshooting sequence is shown in Table 6-16. After running the diagnostics, compare the results with the Diagnostic Test Results column of the table. Follow the procedure for the lowest numbered step where the Diagnostic Test Results match your results when running the diagnostics.

The test numbers are the test numbers associated with each diagnostic. These numbers are displayed with the diagnostic results in the Error Log.

The Error Log is a history of all the diagnostic tests that have been executed since the last time the log was cleared. The Error Log can be accessed as follows:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
UTILITY	SELF TEST	VIEW RESULTS	Page Up (5 times)
		VIEW RESULTS	Error Log

If the problem is occurring regularly, it may be useful to clear the Error Log and then run the diagnostics so that the present error results are easy to see. To clear the Error Log:

Press Menu Button	Select Menu Page	Highlight Parameter	Select Choice
UTILITY	SELF TEST	VIEW RESULTS	Clear
		VIEW RESULTS	Exit

If the problem is intermittent, look at the last entry in the Error Log. Use the Page Down selection to move to the last entry in the Error Log. If the Error Log becomes full, the first entry in the Log (the oldest data) is discarded.

Table 6-16: Troubleshooting Sequence

Step	Diagnostic Test Results	Procedure
1.	BUS FAULT @ 0X9B05XX OR 0X9B0AXX INTERNAL ERROR 1 (SYSTEM EVENT 6) NO OUTPUT FROM CPU RS232 PORT	This combination of failures indicates that the +12 V or -12 V power supply generated by the Backplane board is faulty. Use the Backplane Troubleshooting Procedure to isolate the problem.
2.	No output from CPU RS232 port No +12 V present on U39 pin 1 and U38 pin 1 on the CPU board No -12 V present on U39 pin 8 and U38 pin 8 on the CPU board	This special case is caused by the lack of +12 V and/or -12 V on the RS232 interface chips, U38 and U39. Use the Backplane Troubleshooting procedure to isolate the problem.
3.	No output from CPU RS232 port +12 V present on U39 pin 1 and U38 pin 1 on the CPU board -12 V present on U39 pin 8 and U38 pin 8 on the CPU board	A failure of the RS232 output has the following possible causes(in order of probability): 1. CPU board
4.	CPU tests except Clk/Cal Battery (1, 2, 3, and 5) fail	Failure of any CPU or Processor Diagnostic indicates a failure on the CPU board. The CPU board should be replaced before any other troubleshooting is attempted.
5.	Clk/Cal Battery (4) failure	The most likely cause of a Clk/Cal Battery failure is the Back–Up battery, the cable or connectors from the battery to the CPU board, or the battery has been disconnected and then connected (it could be an intermittent cable). If you know that the battery has been disconnected and then reconnected, then use UTILITY/MISC SETTINGS to set the time and date. After the time and date have been set, power the instrument OFF and then ON. The Clk/Cal Battery failure should not appear. If the failure still appears, replace the CPU board. If the condition of the battery or cable is suspect, replace them, and then set the time and date. After the time and date have been set, power the instrument OFF and then ON. The Clk/Cal Battery failure should not appear. If the failure still appears, replace the CPU board.

6.	Bus fault @ 0x9b05XX or 0x9b0AXX	A bus fault on the ITX(0x9b05XX) or the Hardware Timer (0x9b0AXX) indicates the Tx clock is not present in the system. The Tx Clock gets to the Protocol system from the Clock board. The lack of a Tx clock can be caused by the following items (in order of probability): 1. Cable from Clock board to Main Protocol board 2. High Speed Protocol board 3. Clock board 4. Main Protocol board
7.	Internal error 1 (System Event 6)	This fault is caused by the SETI chip on the High Speed Protocol board not being able to lock to the SETI_REFCLK clock signal. The fault can be caused by the following items (in order of probability): 1. Cable from Clock Board to Main Protocol Board 2. High Speed Protocol board 3. Clock board 4. Main Protocol board
8.	Bus fault @ 0x9b06XX	This failure indicates a problem with the clock for the Rx portion of the Protocol system. The fault can be caused by the following items (in order of probability): 1. If failure is on 52 Mb/s data rate, Plug–In Interface Module 2. High Speed Protocol board 3. Main Protocol board
9.	Any clock board diagnostic fails	This failure indicates a problem with the Clock board circuitry. The fault can be caused by the following items (in order of probability): 1. Clock board 2. Backplane board (low probability) 3. CPU board (low probability)
10.	Bus fault @ 0x9b05XX or 0x9b0AXX Any clock board diagnostic fails	These failures indicate the following possible causes (in order of probability): 1. Clock Board 2. Cable from Clock board to Main Protocol board 3. High Speed Protocol board 4. Main Protocol board
11.	Internal error 1 (System Event 6)	These failures indicate the

	Any clock board diagnostic fails	following possible causes (in order of probability): 1. Clock board 2. Cable from Clock board to Main Protocol board 3. High Speed Protocol board 4. Main Protocol board
12.	Plug–In Interface Module status fails	The system does not detect that a Plug–In Interface Module is installed. The fault can be caused by the following items (in order of probability): 1. Plug–In Interface Module 2. Main Protocol board
13.	Plug–In Interface Module identification (42) fails Plug–In Interface Module access (43) passes	This indicates a failure to read the O/E Identification Register and yet the Plug–In Interface Module Access test passed. The fault is caused by the Plug–In Interface Module.
14.	Plug–In Interface Module identification (42) passes Plug–In Interface Module access (43) fails	This indicates a failure to read and/or write to the Plug–In Interface Module. This indicates a failure to read the O/E Identification Register. The fault is caused by the Plug–In Interface Module.
15.	Plug–In Interface Module identification (42) fails Plug–In Interface Module access (43) fails	This indicates a failure to read the O/E Identification Register and a failure to access the Plug–In Interface Module registers. The fault can be caused by the following items (in order of probability): 1. Plug–In Interface Module 2. 100 pin cable from Display board to Main Protocol board 3. Main Protocol board 4. Backplane board 5. Display board 6. CPU board
16.	Plug–In Interface Module Tx optical power (44) fails Protocol board A/D converter (34) passes	This indicates a failure to obtain a voltage from the Plug–In Interface Module that is within the expected range for the Tx optical power. The fault can be caused by the following items(in order of probability): 1. Plug–In Interface Module

		2. Main Protocol board
17.	Protocol board A/D converter (34) fails	This indicates a failure of the A/D converter on the Main Protocol board to correctly measure the GND and 2.5 V reference signals. The fault is caused by the Main Protocol board.
18.	Protocol board A/D converter (34) passes Plug–In Interface Module Rx optical power (45) fails	This indicates a failure to obtain a voltage from the Plug–In Interface Module that is within the expected range for the Rx optical power. The fault can be caused by the following items (in order of probability): 1. No cable attached for External Loopback 1. Plug–In Interface Module 2. Main Protocol board
19.	Any Display board diagnostics fail	This indicates a failure in the Display board circuitry. The fault can be caused by the following items (in order of probability): 1. Display board 2. Backplane board (low probability) 3. CPU board (low probability)
20.	Any Front Panel diagnostics	This indicates a failure in the Front Panel system. The fault can be caused by the following items (in order of probability): 1. Front Panel board 2. Cable from Front Panel board to CPU board 3. CPU board (very low probability)
21.	Any Display board diagnostics pass Disk Drive diagnostics (14, 15, 16, or 17) fail	These failures indicate a problem with the disk drive electronics. The fault is caused by the Display board.
22.	Any Display board diagnostics pass Disk Drive diagnostics (14, 15, 16, or 17) pass Disk Drive diagnostics (18, 19, or 20) fail	These failures indicate a problem with the physical disk drive. The fault can be caused by the following items (in order of probability): 1. Cable from disk drive to display board 2. Disk drive 3. Display board
23.	Internal error 2 or 3 (system event 7 or 8)	These errors indicate the software system was not able to detect the

		presence of the Main Protocol board. The fault can be caused by the following items (in order of probability): 1. Cable from Display board to Main Protocol board 2. Main Protocol board 3. Display board (low probability) 4. Backplane board (low probability) 5. CPU board (low probability)
24.	Internal event 4 (system event 14)	This error message indicates an error was detected while communicating with the Plug–In Interface Module over the I^2C bus. A better definition of the problem can probably be found by running the Plug–In Interface Module diagnostics #41, #42, and #43 since each of these diagnostics use the I^2C bus to communicate with the Plug–In Interface Module.
25.	Misc Reg (25) fails	This failure indicates a problem writing and/or reading data from the MISC register on the Main Protocol board. The fault can be caused by the following items (in order of probability): 1. Cable from Display board to Main Protocol board 2. Main Protocol board 3. Display board (low probability) 4. Backplane board (low probability) 5. CPU board (low probability)
26.	Misc Reg (25) passes Register access (27) fails	This failure indicates a problem writing or reading data from a number of different registers on the Main and High Speed Protocol boards. The fault can be caused by the following items (in order of probability): 1. Cable from Display board to Main Protocol board 2. Main Protocol board 3. High Speed Protocol board 4. Display board (low probability) 5. Backplane board (low probability)

		6. CPU board (low probability)
27.	FLASH voltage	This indicates the FLASH programming voltage has been left enabled on the Display board. The fault can be caused by the following items (in order of probability): 1. Protocol board Programming Enable switch on the Display board is left in ON position 2. Cable from Display board to Main Protocol board 3. Main Protocol board 4. Display board (low probability)
28.	Register access (27) passes FLASH checksum (29) fails	This indicates the checksum calculated for the FLASH on the Main Protocol board does not agree with the checksum stored in the FLASH. The fault can be caused by the following items (in order of probability): 1. Main Protocol board 2. Display board (low probability)
29.	Register access (27) passes ITX RAM (30) fails	This indicates a failure occurred while trying to write and/or read the ITX RAM on the High Speed Protocol board. The fault is caused by the High Speed Protocol board.
30.	Register access (27) passes IRX RAM (31) fails	This indicates a failure occurred while trying to write and/or read the IRX RAM on the High Speed Protocol board. The fault is caused by the High Speed Protocol board.
31.	Register access (27) passes PRX RAM (32) fails	This indicates a failure occurred while trying to write and/or read the PRX RAM on the Main Protocol board. The fault is caused by the Main Protocol board.
32.	Register access (27) passes IRX RAM (31) passes IRX FIFO (33) fails	This indicates a failure occurred while trying to write and/or read the IRX FIFO on the High Speed Protocol board. The fault is caused by the High Speed Protocol board.
33.	Power supply (33) fails	This indicates that one or more of the power supplies generated on the Main Protocol board is not at its expected voltage. The fault can be caused by the following items (in order of probability):

		1. Plug–In Interface Module 2. High Speed Protocol board 3. Main Protocol board 4. Low Voltage Power Supply
34.	Protocol board 52, 155, 622 Mb/s loop (36, 37, and 38) passes Plug–In Interface Module 52, 155, 622 Mb/s internal loop (46, 47, or 48) fails	This indicates one or more failures were detected when looping the Tx signal back to the Rx, within the Plug–In Interface Module. These faults can be caused by the following items (in order of probability): 1. Plug–In Interface Module 2. High Speed Protocol board 3. Main Protocol board (low probability)
35.	Protocol board 52, 155, 622 Mb/s loop (36, 37, and 38) passes Plug–In Interface Module 52, 155, 622 Mb/s internal loop (46, 47, and 48) passes Plug–In Interface Module 52, 155, 622 Mb/s external loop (49, 50, and 51) fails	This indicates one or more failures were detected when looping the Tx signal back to the Rx through external cables. These faults can be caused by the following items (in order of probability): 1. External cables not attached or not connected properly 2. If the failures only involve Optical signals, the problem may be dirty optical cables or connectors 3. Plug–In Interface Module 4. Main Protocol board (low probability)
36.	Protocol board 52, 155, 622 Mb/s loop (36, 37, or 38) fails Fails with B1 and/or B2 errors detected but not inserted	This indicates one or more failures were detected when looping the Tx signal back to the Rx on the High Speed Protocol Board. These faults can be caused by the following items (in order of probability): 1. High Speed Protocol board 2. Main Protocol board 3. Clock Generator board
37.	Protocol board 52, 155, 622 Mb/s loop (36, 37, or 38) fails Does not fail with B1 and/or B2 errors detected but not inserted Fails with B3 errors detected when not inserted	This indicates one or more failures were detected when looping the Tx signal back to the Rx on the High Speed Protocol Board. Since there are B3 errors but no B1 and/or B2 errors, the following items (in order of probability) should be checked: 1. Main Protocol board 2. High Speed Protocol board (low probability) 3. Clock Generator board (low probability)

38.	Protocol board 52, 155, 622 Mb/s loop (36, 37, or 38) fails Does not fail with B1 and/or B2 errors detected but not inserted Does not fail with B3 errors detected when not inserted Fails with Pattern Loss detected	This indicates one or more failures were detected when looping the Tx signal back to the Rx on the High Speed Protocol board. Since there are no B3 errors but there is a Pattern Loss, the problem is most likely in the Path processing on the Main Protocol board. If, however, there is only a single occurrence of a Loss of Pattern when the system is allowed to loop on diagnostics for several hundred passes, then the most likely failure is the frame pulse generated from the STTX on the High Speed Protocol board. This is a failure mode that is only activated by the diagnostic loop and causes no problem in normal operation. This single occurrence failure should be ignored and no repair attempted. If the problem is persistent Loss of Pattern, then the following items (in order of probability) should be checked: 1. Main Protocol board 2. High Speed Protocol board 3. Clock Generator board (low probability)
39.	Protocol board 52, 155, 622 Mb/s loop (36, 37, or 38) fails Does not fail with B1 and/or B2 errors detected but not inserted Does not fail with B3 errors detected when not inserted Does not fail with Pattern Loss detected Fails with B1 and/or B2 errors inserted but not detected	This indicates the diagnostics tried to insert errors, but no errors were detected when looping the Tx signal back to the Rx on the High Speed Protocol board. Since the diagnostics stop when finding a B1 or B2 error, the condition of the B3 error insertion is unknown. But since no other problems were found with the B1 and/or B2 functions, it is more likely that the problem is with the error insertion function which is done through the Hardware Timer module on the Main Protocol board. The following items (in order of probability) should be checked: 1. Main Protocol board 2. High Speed Protocol board 3. Clock Generator board (low probability)
40.	Protocol board 52, 155, 622 Mb/s loop (36, 37, or 38) fails Does not fail with B1 and/or B2 errors detected but not inserted Does not fail with B3 errors	This indicates the diagnostics tried to insert errors, but no errors were detected when looping the Tx signal back to the Rx on the High Speed Protocol board. Since

	detected when not inserted Does not fail with Pattern Loss detected Does not fails with B1 and/or B2 errors inserted but not detected Fails with B3 errors inserted but not detected	problems were found only in the B3 error function, the Main Protocol board is the most likely candidate since all B3 error insertion functions are on the Main Protocol board. The following items (in order of probability) should be checked: 1. Main Protocol board 2. High Speed Protocol board 3. Clock Generator board (low probability)
41.	Protocol board 52, 155, 622 Mb/s loop (36, 37, or 38) fails Does not fail with B1 and/or B2 errors detected but not inserted Does not fail with B3 errors detected when not inserted Does not fail with Pattern Loss detected Does not fail with B1 and/or B2 errors inserted but not detected Does not fail with B3 errors inserted but not detected Fails positive and/or negative pointer movements	Since all Pointer Processing functions for the Protocol Board diagnostics are on the Main Protocol board, the Main Protocol board is the most likely cause of the problem. The following items (in order of probability) should be checked: 1. Main Protocol board 2. Clock Generator board (low probability)
42.	Protocol board 52, 155, 622 Mb/s loop (36, 37, or 38) fails Fails STS–3/OC–3/OC–12 only with STS–3c structure	The diagnostics tests STS–3, OC–3, and OC–12 operation with both STS–1 and STS–3c structure. If problems are found only in STS–3c structure, the most likely cause is the Main Protocol board which generates the Path level information. The problem can also be in the High Speed Protocol board where the Path level clock signal originates. The following items (in order of probability) should be checked: 1. Main Protocol board 2. High Speed Protocol board 3. Clock Generator board (low probability)
43.	Protocol board 52, 155, 622 Mb/s loop (36, 37, or 38) fails Fails with LOS and/or LOF detected	This failure indicates that an LOS or LOF failure was detected at some time during the diagnostic when it was not expected. The following items (in order of probability) should be checked: 1. High Speed Protocol board 2. Main Protocol board (low probability) 3. Clock Generator board (low probability)

44.	JAWA/JAWG Option 14 is installed but not recognized by the CTS 750. The message " Jitter/Wander Option Not Installed" is displayed.	Verify correct connection of all cables to the JAWA/JAWG assembly, in particular, the short coaxial cable to the Clock Generator board.
45.	Jitter fails to calibrate at STM0.	Verify that the two cables from the JAWA/JAWG assembly to the Protocol board are installed correctly.
46.	Jitter fails to calibrate at one of the tributary rates.	Verify that the cables from the JAWA/JAWG assembly to the Tributary assembly are installed correctly. The following items (in order of probability) should be checked: 1. Tributary Assembly
47.	JAWA/JAWG diagnostic codes fail (78 through 97)	Verify correct connection of all cables to the JAWA/JAWG assembly. The following items (in order of probability) should be checked: 1. JAWA/JAWG assembly 2. Tributary Assembly 3. Clock Generator board

Example of Fault Isolation

The following results were obtained from running the System External and System Internal diagnostics.

After running the System External diagnostics:

```
O/E Ext 155 Mb Loop Elec 155 Mb
          LOS Exp:0x0 Act:0x1

O/E Ext 622 Mb Loop Opt 622 Mb
          LOS Exp:0x0 Act:0x1
```

These External loopback diagnostics are interpreted as follows:

```
O/E Ext    --- module name: Plug–In Interface
Module with External Loop 155 Mb Loop Elec
155 Mb: type of diag run
LOS        --- type of failure: Loss of
Signal(LOS)
Exp:0x0    --- expected value: 0 (no LOS
present)
Act:0x1    --- actual value: 1 (LOS was
present)
```

After running the System Internal diagnostics:

```
O/E Int 155 Mb Loop Elec 155 Mb
          LOS Exp:0x0 Act:0x1
```

```
O/E Int 622 Mb Loop Opt 622 Mb
          LOS Exp:0x0 Act:0x1
```

The Internal diagnostic results are interpreted the same as the External diagnostics with the module name changed to O/E Int.

After running the Protocol Board diagnostics:

```
Proto Bd 155 Mb Loop Elec 155 Mb
          LOS Exp:0x0 Act:0x1

Proto Bd 622 Mb Loop Opt 622 Mb
          LOS Exp:0x0 Act:0x1
```

The Protocol board diagnostic results are interpreted the same as the External diagnostics with the module name changed to Proto Bd.

Match these results against the Troubleshooting Sequence table. (Failures occurred in the Plug–In Interface Module Internal and External tests, and in the Protocol Board Loopback test.) The best match for these diagnostic results is at step 43.

Step 43 lists the following boards as possible suspects:

1. High Speed Protocol board
2. Main Protocol board (low probability)
3. Clock Generator board (low probability)

Since the High Speed Protocol board is listed as the highest probability for causing the problem, replace this board first. The High Speed and Main Protocol boards are considered a single unit and should be replaced as a single unit. After replacing the High Speed Protocol board, run all of the diagnostics again.

If there are no diagnostic failures after replacing a board, the Protocol boards were faulty. If the same diagnostic failures occur, the original Protocol boards should be reinstalled and the Clock Generator board should be replaced. After replacing the Clock Generator board, all the diagnostics should be run again.

If there are no diagnostic failures, the Clock Generator board was at fault. If the same diagnostic failures occur, the original Clock Generator board should be replaced in the instrument. Since all of the suggested sources of problems have been tested and the problem still remains, the instrument should be returned to the factory for service. A complete history of all attempts at problem resolution should be sent along with the instrument.

Troubleshooting Notes

Bus Faults can occur during any diagnostic. These faults are characterized by the following message:

```
BUS ERROR At Addr: 0xXXXXXX, (STTX Reg 3:
0xXX)
```

If a message like the above appears in any diagnostic failure display, it should be treated as a bus fault and not as a failure by the specific diagnostic.

If you have a large number of diagnostic failures, verify that the Low Voltage Power Supply is working.

You can run all of the diagnostics in loops to help isolate intermittent problems. Since some circuitry only produces failures under temperature stress, run the diagnostics at the same temperature that is causing the problems.

The entries in the Troubleshooting Sequence procedure are listed in order of probability of causing a problem.

After–Repair Adjustments

After the removal and replacement of a module, some adjustment may be required. Table 6-17 lists the adjustments required.

Table 6-17: Adjustments Required for Module Replaced

Module Replaced	Adjustment Required
Display Assembly	None required
Backplane Assembly	None required
CPU Assembly	Set the clock and calendar
Auxiliary Power Supply	None required
Clock Generator Assembly	None required
Main Protocol Assembly	Set the serial number
High Speed Protocol Assembly	None required
Tributary Assembly	Calibrate Jitter (if option 14 is installed)
JAWA/JAWG Assemby	Calibrate Jitter
Optical or Electrical Interface Module	Calibrate Jitter (if option 14 is installed)
Low Voltage Power Supply	Adjust the display monitor
Monitor Assembly	Adjust the display monitor

Repackaging Instructions

If you ship the CTS, pack it in the original shipping carton and packing material. If the original packing material is not available, package the CTS as follows:

1. Obtain a corrugated cardboard shipping carton with inside dimensions at least 15 cm (6 in) taller, wider, and deeper than the CTS. The shipping carton must be constructed of cardboard with 170 kg (375 pound) test strength.
2. If you are shipping the CTS to a Tektronix field office for repair, attach a tag to the CTS showing its owner and address, the name of the person to contact about the CTS, the CTS type, and the serial number.
3. Wrap the CTS with polyethylene sheeting or equivalent material to protect the finish.
4. Cushion the CTS in the shipping carton by tightly packing dunnage or urethane foam on all sides between the carton and the CTS. Allow 7.5 cm (3 in) on all sides, top, and bottom.
5. Seal the shipping carton with shipping tape or an industrial stapler.

Options

Table 7-1 below lists the options you may find installed in the CTS850 SDH/PDH Test Set.

Table 7-1: CTS850 SDH/PDH Test Set Options

Option	Description
Option 01	STM-0/1E 51/155 Mbit/s Electrical Interface Plug-in
Option 03	Optical and Electrical 1310 nm Interface Plug-in for 52 Mbit/s and 155 Mbit/s
Option 04	Optical and Electrical 1310 nm Interface Plug-in for 52 Mbit/s, 155 Mbit/s, and 622 Mbit/s
Option 05	Optical and Electrical 1550 nm Interface Plug-in for 52 Mbit/s, 155 Mbit/s, and 622 Mbit/s
Option 06	Optical and Electrical 1310/1550 nm Interface Plug-in for 52 Mbit/s, 155 Mbit/s, and 622 Mbit/s (combines Opt 04 and Opt 05)
Option 08	VC4-4c concatenated 622 Mbit/s mapping
Option 12	1.6/5.6 connectors for all 75 ohm BNC front panel connectors
Option 14	SDH/PDH Jitter/Wander Test, including Wander Analyst application software for a Personal Computer
Option 31	FC-PC connector sub-option for O/E modules (optional extras for Options 03, 04, 05, and 06)
Option 32	ST connector sub-option for O/E modules (optional extras for Options 03, 04, 05, and 06)
Option 33	SC connector sub-option for O/E modules (optional extras for Options 03, 04, 05, and 06)
Option 34	DIN connector sub-option for O/E modules (optional extras for Options 03, 04, 05, and 06)
Option 38	Nx64kbit/s, 2 Mbit/s, 8 Mbit/s, 34 Mbit/s, 140 Mbit/s, TU-12, TU3 Capabilities Includes: Electrical interface for 2 Mbit/s, 8 Mbit/s, 34 Mbit/s, and 140 Mbit/s plus Mux/Demux front panel connectors; 120 Ω 3-pin Siemens, 75 Ω BNC

Note: Any options that are not listed in the tables above are not supported by this manual and must be returned to the factory for all servicing.

In addition, the following items can be ordered by their nine-digit Tektronix part numbers:

Accessories:

- ◊ 10dB attenuator (FC-PC to FC-PC) - Part #119-1387-00
- ◊ Connector Kit (FC-PC, ST, DIN, & SC) - Part #020-1885-00
- ◊ Rack mount Kit (19”) - Part #016-1406-xx
- ◊ Printer - HC411 Thermal Printer
- ◊ Hard Case - Part #016-1157-00
- ◊ Soft Case - Part #016-1158-00
- ◊ Adapter BNC, 1.6/5.6 - Part #013-0300-00
- ◊ CTS850 User Manual - Part #070-9988-xx
- ◊ CTS850 Programmer Manual - Part #070-9990-xx

Cables:

Single Mode Optical Cables

- ◊ FC-PC to FC-PC, 2 m - Part #174-1387-00
- ◊ FC-PC to ST, 2 m - Part #174-1386-00
- ◊ FC-PC to Biconic, , 2 m - Part #174-1388-00
- ◊ FC-PC to Diamond 3.5, 2 m - Part #174-1385-00

Electrical Cables

- ◊ 2 Mbit/s Siemens-Siemens, 120 Ω, 2 m - Part #012-1469-00
- ◊ PDH/STM-1E BNC-BNC, 75 Ω, 2 m - Part #012-1338-00

For information about power cord options, refer to Table 2-2, in Section 2 of this manual.

Electrical Parts List

The modules that make up this instrument are often a combination of mechanical and electrical subparts. Therefore, all replaceable modules are listed in the *Mechanical Parts List* section. Refer to that section for part numbers when using this manual.

Diagrams

This section contains an interconnect diagram and a block diagram for the CTS850. Refer to Section 3, *Theory of Operation*, for more information about the field–replaceable modules shown in the block diagram.

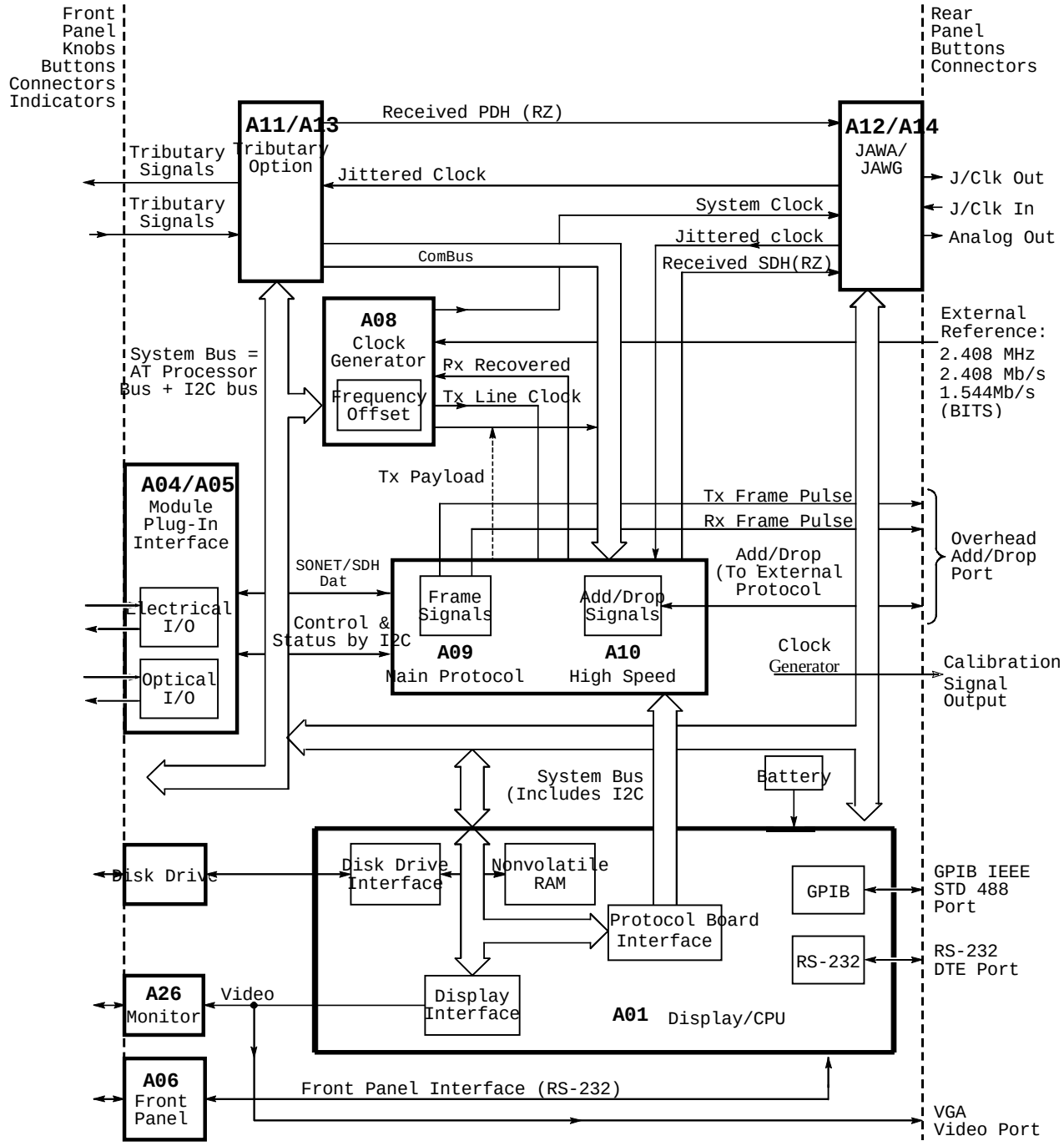


Figure 9-1: CTS Block Diagram

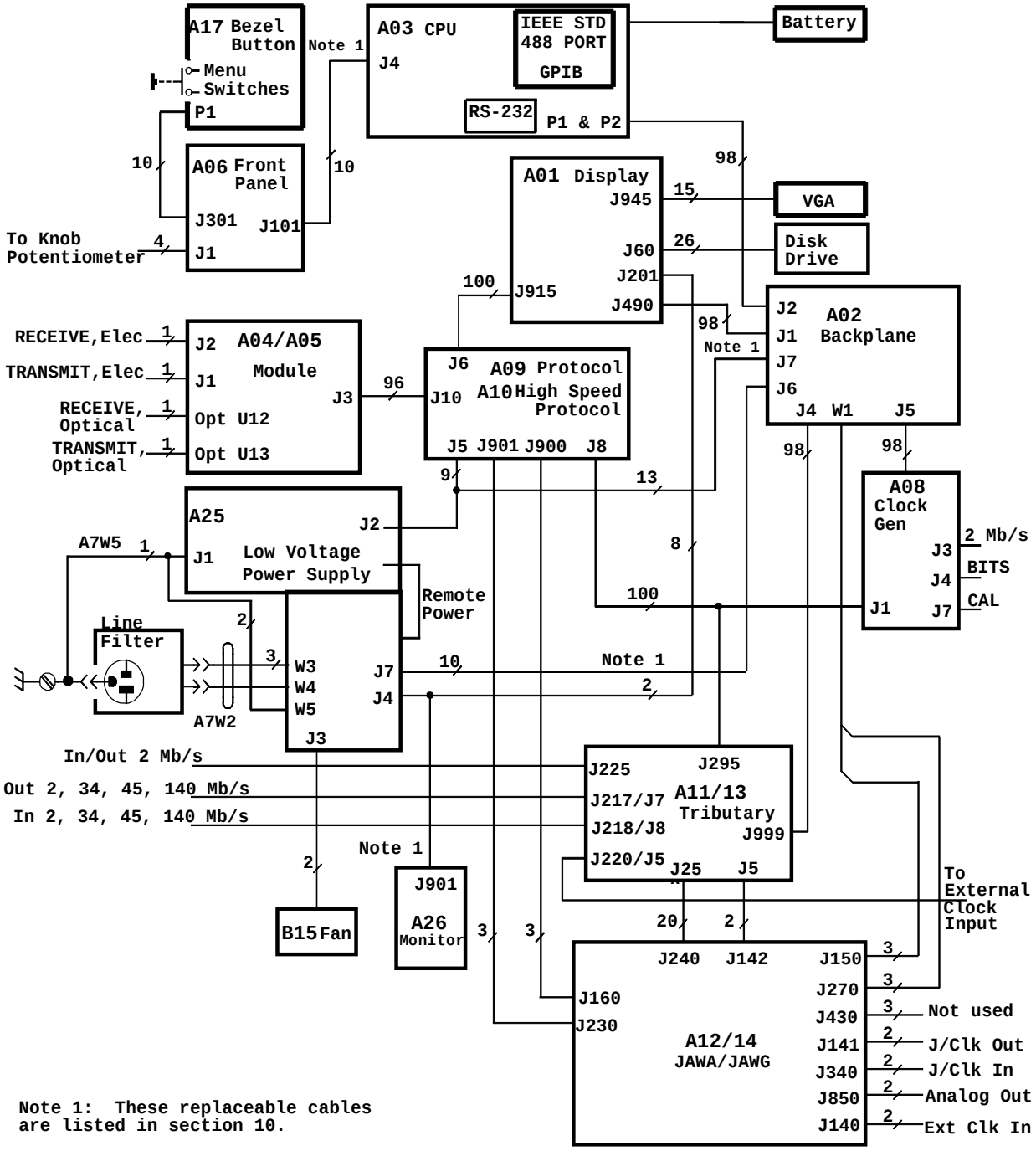


Figure 9-2: CTS Interconnect Diagram

Mechanical Parts List

This section contains a list of the modules that are replaceable for the CTS. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available from or through your local Tektronix, Inc. service center or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest circuit improvements. Therefore, when ordering parts, it is important to include the following information in your order.

- ⇒ Part number
- ⇒ Instrument type or model number
- ⇒ Instrument serial number
- ⇒ Instrument modification number, if applicable

If a part you order has been replaced with a different or improved part, your local Tektronix service center or representative will contact you concerning any change in the part number.

Change information, if any, is located at the rear of this manual.

Module Replacement

The CTS is serviced by module replacement so there are three options you should consider:

- ⇒ **Module Exchange.** In some cases you may exchange your module for a remanufactured module. These modules cost significantly less than new modules and meet the same factory specifications. For more information about the module exchange program, call 1-800-TEKWIDE, ext. 6630.
- ⇒ **Module Repair.** You may ship your module to us for repair, after which we will return it to you.

⇒ **New Modules.** You may purchase new replacement modules in the same way as other replacement parts.

Using the Replaceable Parts List

The tabular information in the parts list is arranged for quick retrieval. Understanding the structure and features of the list will help you find all the information you need for ordering replacement parts.

Item Names

In the parts list, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, U.S. Federal Cataloging Handbook H6-1 can be used where possible.

Indentation System

This parts list is indented to show the relationship between items. The following example is of the indentation system used in the Description column:

1 2 3 4 5 Name & Description
Assembly and/or Component
Attaching parts for Assembly and/or Component
(END ATTACHING PARTS)
Detail Part of Assembly and/or Component
Attaching parts for Detail Part
(END ATTACHING PARTS)
Parts of Detail Part
Attaching parts for Parts of Detail Part
(END ATTACHING PARTS)

Attaching parts always appear at the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation. Attaching parts must be purchased separately, unless otherwise specified.

Abbreviations

Abbreviations conform to American National Standards Institute (ANSI) standard Y1.1.

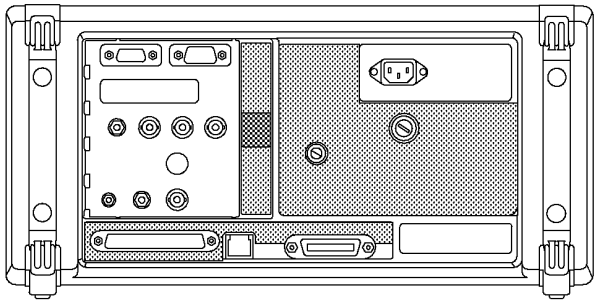
CROSS INDEX - MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip Code
S3109	FELLER	72 VERONICA AVE UNIT 4	SUMMERSET NJ 08873
S3629	SCHURTER AG H C/O PANEL COMPONENTS CORP	2015 SECOND STREET	BERKLEY CA 94170
S4246	JAPAN SERVO CO LTD	7 KANDA MITOSHIRO-CHO CHIYODA-KU	TOKYO JAPAN
TK0435	LEWIS SCREW CO	4300 S RACINE AVE	CHICAGO IL 60609-3320
TK0860	LABEL GRAPHICS	6700 SW BRADBURY CT	PORTLAND OR 97224
TK1163	POLYCAST INC	9898 SW TIGARD ST	TIGARD OR 97223
TK1547	MOORE ELECTRONICS INC	19500 SW 90TH CT PO BOX 1030	TUALATIN OR 97062
TK1694	ROSE CITY LABEL COMPANY	7235 SE LABEL LANE	PORTLAND OR 972069339
TK1857	HIROSE ELECTRIC USA INC	2688 WESTHILLS COURT	SIMI VALLEY CA 93065-6235
TK1891	PRESTOLE CORP	34589 GLENDALE ST	LIVONIA MI 48150-1303
TK1908	PLASTIC MOLDED PRODUCTS	4336 SO ADAMS	TACOMA WA 98409
TK1918	SHIN-ETSU POLYMER AMERICA INC	1181 NORTH 4TH ST	SAN JOSE CA 95112
TK1935	ACCRA-FAB INC	11007 NE 37TH CIRCLE	VANCOUVER WA 98682
TK1943	NEILSEN MANUFACTURING INC	3501 PORTLAND ROAD NE	SALEM OR 97303
TK2248	WESTERN MICRO TECHNOLOGY	1800 NW 169TH PL SUITE B-300	BEAVERTON OR 97006
TK2432	UNION ELECTRIC	15/F #1, FU-SHING N. ROAD	TAIPEI TAIWAN ROC
TK2469	UNITREK CORPORATION	3000 LEWIS & CLARK WAY SUITE #2	VANCOUVER WA 98601
TK2539	ROYAL CASE COMPANY INC	315 S MONTGOMERY PO BOX 2231	SHERMAN TX 75070
TK2548	XEROX BUSINESS SERVICES DIV OF XEROX CORPORATION	14181 SW MILLIKAN WAY	BEAVERTON OR 97077
TK2647	INSTRUMENT SPECIALTIES CO INC.	C/O TEMCO NW 1336 SE 51ST STREET	HILLSBORO OR 97123
TK6122	SELECTRON INC	7225 SW BONITA	TIGARD OR 97224
0D1M6	NMB TECHNOLOGIES INC	9730 INDEPENDENCE AVE	CHATSWORTH CA 91311
0DWW6	SPM/MICRO POWER ELECTRONICS	22990 NW BENNETT ST	HILLSBORO OR 97124
0DWW6	MICRO POWER ELECTRONICS	7973 SW CIRRUS DRIVE BLDG. #22	BEAVERTON OR 97005
0GV52	SCHAFFNER EMC INC	9-B FADEM ROAD	SPRINGFIELD NJ 07081
0JR05	TRIQUEST CORP	3000 LEWIS AND CLARK HWY	VANCOUVER WA 98661-2999
0KBZ5	Q & D PLASTICS INC	1812 - 16TH AVENUE PO BOX 487	FOREST GROVE OR 97116-0487
0KBZ5	MORELLIS Q & D PLASTICS	1812 16TH AVE	FOREST GROVE OR 97116
0KB01	STAUFFER SUPPLY CO	810 SE SHERMAN	PORTLAND OR 97214-4657
0KB05	NORTH STAR NAMEPLATE INC	5750 NE MOORE COURT	HILLSBORO OR 97124-6474
0KM03	INSTRUMENT SPECIALTIES CO INC.	505 PORTER WAY	PLACENTIA, CA 92670
00PZ4	EAC SHIELDING	13620 IMPERIAL HWY UNIT #7	SANTA FE SPRING CA 90670

CROSS INDEX - MFR. CODE NUMBER TO MANUFACTURER (continued)

Mfr. Code	Manufacturer	Address	City, State, Zip Code
00779	AMP INC.	CUSTOMER SERVICE DEPT PO BOX 3608	HARRISBURG PA 17105-3608
060D9	UNITREK CORPORATION	3000 COLUMBIA HOUSE BLVD SUITE 120	VANCOUVER, WA 98661
07416	NELSON NAME PLATE CO	3191 CASITAS	LOS ANGELES CA 90039-2410
1AW87	LEWIS SCREW CO	4300 SOUTH RACINE AVENUE	CHICAGO IL 60609
1DM20	PARLEX CORP	7 INDUSTRIAL WAY	SALEM NH 03079
1JJ96	KAM ELECTRIC CO	11866 SLATER AVENUE NE	KIRKLAND WA 98034
14949	TROMPETER ELECTRONICS INC	31186 LA BAYA DR	WESTLAKE VILLAGE CA 91362-5069
18565	CHOMERICS INC	77 DRAGON COURT	WOBURN MA 01801-1039
2K262	BOYD CORPORATION	6136 NE 87th AVENUE	PORTLAND OR 97220
2W733	COOPER INDUSTRIES INC BELDEN DIVISION	2200 US HIGHWAY 27 SOUTH PO BOX 1980	RICHMOND IN 47375-0010
22670	GM NAMEPLATE INCORPORATED	2040 15TH AVE WEST	SEATTLE WA 98119-2783
26003	MODULAR DEVICES INC	4115 SPENCER STREET	TORRANCE CA 90503-2489
30817	INSTRUMENT SPECIALTIES CO INC	SHIELDING WAY PO BOX A	DELAWARE WATER GAP PA 18327
3A054	MCMASTER-CARR SUPPLY CO	9630 NORWALK BLVD	SANTA FE SPRINGS CA 90670
34416	PARSONS MFG CORP	1055 OBRIAN DR	MENLO PARK CA 94025-1408
50356	TEAC AMERICA INC	7733 TELEGRAPH RD PO BOX 750	MONTEBELLO CA 90640-6537
50463	POWER SYSTEMS INC.	45 GRIFIN ROAD	SOUTH LINFIELD CT 06002
53387	3M COMPANY ELECTRONIC PRODUCTS DIV	3M AUSTIN CENTER	AUSTIN TX 78769-2963
56501	THOMAS & BETTS CORPORATION	1555 LINFIELD RD	MEMPHIS TN 38119
59730	THOMAS AND BETTS CORP	1555 LINFIELD RD	MEMPHIS TN 38141
61857	SAN-0 INDUSTRIAL CORP	91-3 COLIN DRIVE	HOLBROOK NY 11741
61935	SCHURTER INC	1016 CLEGG COURT	PETALUMA CA 94952-1152
7X318	KASO PLASTICS INC	5720-C NE 121ST AVE, STE 110	VANCOUVER, WA 98682
70674	ADC PRODUCTS DIV MAGNETC CONTROLS CO		
71400	BUSSMANN	DIVISION COOPER INDUSTRIES INC PO BOX 14460	ST LOUIS MO 63178
74594	COMPONENT RESOURCES INC BUSSMAN PARTS c/o CASEY LAKEY	14525 SW WALKER ROAD	BEAVERTON OR 97006
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON OR 97077-0001
93907	CAMCAR DIV OF TEXTRON INC ATTN: ALICIA SANFORD	516 18TH AVENUE	ROCKFORD IL 61104-5181

Fig. & Index No.	Tektronix Part No.	Serial No. Effective Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
10-1						
-1	390-1171-00		1	CABINET,SCOPE:W/FOOT & SHIELDING	80009	390-1171-00
-2	348-0764-04		1	SHLD GSKT,ELEK:0.125 X 0.188,WIRE MESH,2LAYERS,37L	18565	ORDER BY DESC
-3	200-4324-00		1	COVER,PANEL:HARD, POLYCARBONATE, LEXAN	80009	200-4324-00
-4	334-9393-00		1	MARKER,IDENT:REAR COVER FUSE DATA W/ CE LABEL	80009	334-9393-00
-5	334-9377-00		1	MARKER, IDENT: OPTION GENERIC	80009	334-9377-00
-6	334-9526-00		1	MARKER, IDENT: ANALOG JITTER OUT	80009	334-9526-00
-7	334-9376-00		1	MARKER,IDENT: REAR COVER OVERHEAD ADD DROP	80009	334-9376-00
-8	211-0691-00		4	SCREW,MACHINE:6-32 X 0.625,PNH,STL	0KB01	ORDER BY DESC
-9	367-0497-00		1	HANDLE, CARRYING	80009	367-0497-00
-10	212-0144-00		2	SCREW,TPG,TF:8-16 X 0.562,PLASTITE,SPCL HD	0KB01	ORDER BY DESC
-11	348-0659-00		2	FOOT,CABINET:BLACK POLYURETHANE	0JR05	ORDER BY DESC
-12	211-0730-00		1	SCR,ASSEM WSHR:6-32X0.375 PNH STL CD PL	0KB01	ORDER BY DESC



View showing location of rear panel labels

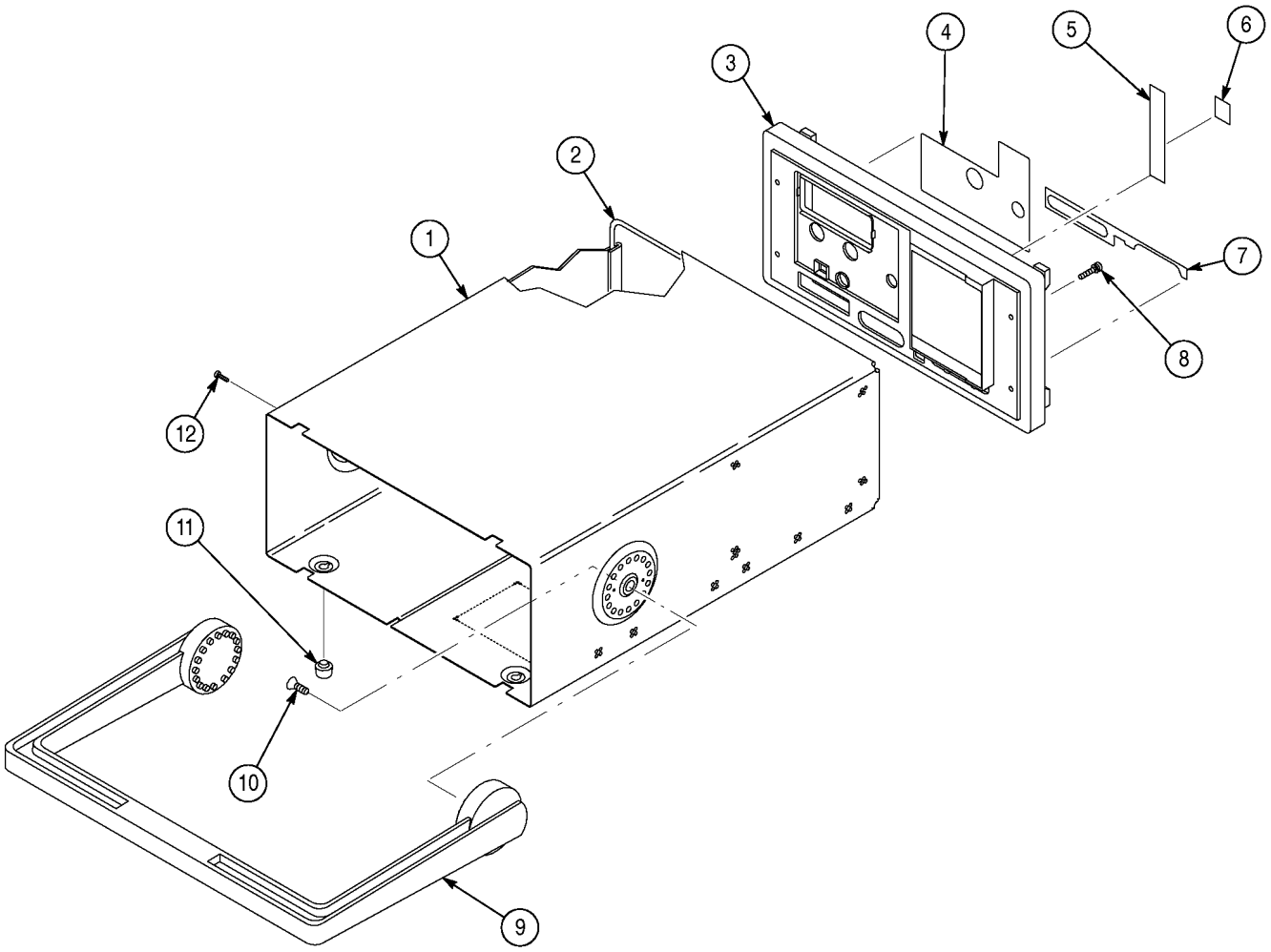


Figure 10-1: Cabinet and Rear Panel

Fig. & Index No.	Tektronix Part No.	Serial No. Effective Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
10-2						
-1	334-9378-00		1	MARKER, IDENT:BEZEL CTS850	80009	334937800
-2	354-0750-00		1	TRIM,RING	TK1163	
-3	354-0750-00		1	TRIM RING: FRONT, W/ACRYLIC CRT FILTER	TK1163	354-0750-00
-4	366-2176-00		12	PUSH BUTTON:MENU BUTTON	TK1163	ORDER BY DESC
	366-0752-00		1	PUSH BUTTON:MENU BUTTON W/ TEXT	TK1163	
-5	260-2539-00		1	SWITCH,SET:;ELASTOMERIC BEZEL	TK1918	260-2539-00
-6	259-0086-00		1	FLEX CIRCUIT:BEZEL BUTTON	07416	ORDER BY DESC
-7	211-0101-001		2	SCREW,MACHINE:4-40X0.25,POZ	93907	ORDER BY DESC
-8	119-5677-00		1	DISK DRIVE	50356	FD-04HF-2300
-9	407-4611-00		1	CTS850, BRACKET	TK1943	407461100
-10	253-0176-00		1	TAPE, PRESS:VINYL FOAM, 0.5x0.062	8009	ORDER BY DESC
-11	276-0849-00		2	CORE, EM: EMI SUPPRESS	11JJ96	ORDER BY DESC
-12	213-0882-00		1	SCREW,TPG,TR:6-32x0.437,T-15 TORX	0KB01	ORDER BY DESC
-13	366-2159-01		1	KNOB	TK1163	366215901
-14	672-0375-51		1	FRONT PANEL CKT BD ASSY	80009	672037551
	672-0381-52		1	FPANEL MODULE OPT. 38	80009	672038152
-15	679-4468-00		1	CKT BD SUBASSY: 2MB/E1, CTS850	80009	679-4468-00
-16	212-0217-00		4	SCREW, MACHINE: 10-32 x 0.25	3A054	91794A825
-17	211-0033-00		2	SCR,ASSEM WSHR: 4-40x0.312, W/EXT LK WSHR	1AW87	ORDER BY DESC
-18	344-0551-00		10	CLIP,EMI:FINGER,0.0035THK,16 IN L	30817	0077-021-19
-19	348-1408-00		1	GASKET,SHIELD:EMI,CLIP-ON,8.5L	80009	348140800
-20	366-0788-00		24	KEYCAP:PUSH BUTTON	TK1163	366078800
-21	174-3368-00		1	CABLE, ASSY, RF: COAXIAL	53387	174336800
	174-3718-00		1	CABLE, ASSY, RF: DISCRETE	060D9	ORDER BY DESC
-22	334-8677-00		1	MARKER, IDENT: CAUTION, LASER	0KB05	334-8677-00
-23	672-1485-52*		1	OPT/ELECTRICAL MODULE	80009	672148552
	672-1486-52*		1	OPT/ELECTRICAL MODULE, OPT 03	80009	672148652
	672-1487-52*		1	OPT/ELECTRICAL MODULE, OPT 06	80009	672148752
	672-1488-52*		1	OPT/ELECTRICAL MODULE, OPT 05	80009	672148852
-24	200-3091-00		2	COVER, DUST: W/BEAD CHAIN, FC STYLE	TK1857	HRFC-C1
-25	348-1409-00		3	CTS710 EMI SHIELD GASKET	00PZ4	348140900
-26	200-4383-00		1	CTS850: COVER, FRONT	7X318	200438300

*When an Opt/Electrical Module is ordered, the appropriate connector option must also be ordered. The connector options are FC connectors (PN 650-3991-00), ST connectors (PN 650-3993-00), SC connectors (PN 650-3994-00), and Din connectors (PN 650-3995-00).

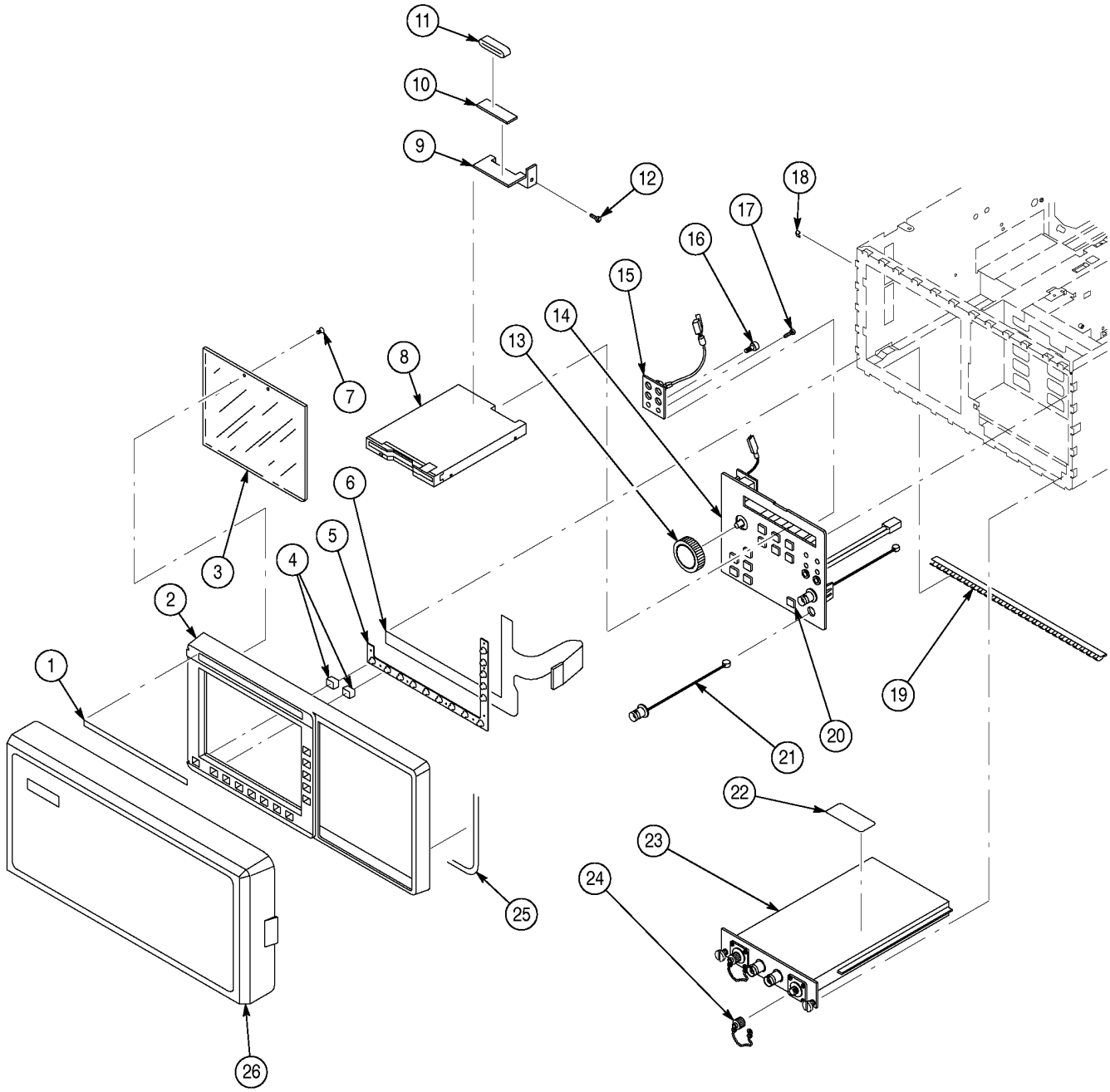


Figure 10-2: Front Panel

Fig. & Index No.	Tektronix Part No.	Serial No. Effective Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
10-3						
-1	407-4491-00		1	CTSxx, BAFFLE,AIR	TK1935	407449100
-2	213-0978-00		1	SCREW,TPG,TR:6-32x0.500,T-10 TORX	0KB01	ORDER BY DESC
-3	213-0882-00			SCREW,TPG,TR:6-32 X 0.437,PNH, STL,CDPL,TYPETT	0KB01	ORDER BY DESC
-4	426-2426-00		1	FRAME,FAN MTG:POLYCARBONATE	TK1163	426-2426-00
-5	119-5602-00		1	FAN,DC:TUBEAXIAL, 12V, 6.84W, 90 CFM, 39 DBA,	0D1M6	DC 4710NL-04W-B50-D00
-6	119-5557-01		1	POWER SUPPLY:225W	26003	119-5557-00
-7	386-6159-00		1	SUPPORT,CKT BD:BACK PLANE & PWR SPLY,PC	TK1163	386-6159-00
-8	159-0046-00		1	FUSE, CARTRIDGE; 3AG, 8A, 250V	71400	ABC 8
-9	119-5807-00		1	BRACKET ASSY, CTS850	80009	119580700
-10	211-0722-00			SCREW,MACHINE:6-32 X 0.250,PNH,STL,CDPL,T-15	0KB01	ORDER BY DESC
-11	213-1079-00		1	JACKSCREW:4-40x0.250 EXT THD	00779	745563-2
-12	407-4637-00		1	BRACKET:CTS850	TK1935	407463700
-13	386-6158-00		3	SUPPORT,CKT BD:MAT MATERIAL	80009	386615800
-14	146-0056-02		1	BATTERY:3V,1200MAH,2/3A LITHIUM BATTERY ASSY,6.250	0DWW6	ORDER BY DESC
-15	344-0116-00		1	RTNR,CAPACITOR:0.625 DIA,STEEL	TK1891	E50003-007
-16	344-0555-00		1	CLIP,GROUND:STRANDED WIRE,CTS850	74594	8182-84-00
-17	671-4009-50		1	CIRCUIT BD:LO-SPEED PROTOCOL	80009	671400950
-18	129-0851-00		5	SPACER,POST:0.709 L	0KB01	129-0851-00
-19	671-4109-50		1	CIRCUIT BD:HI-SPEED PROTOCOL	80009	671410950
-20	348-1412-00		1	GASKET,EMI:W/ADHESIVE	30817	348-1412-00
-21	348-1552-00		1	GASKET,EMI:LONGITUDINAL GND STRIP,COPPER,3.906 L,CLIP ON	TK2647	0097097617 CUT TO 3.906L
-22	348-1620-00		1	SHLD GSKT,ELEC:CLIP-ON PERP,5.0L	30817	9765519049
-23	174-3723-00		1	CA ASSY,SP:SHLD CMPST,SPEAKER, 13.5 L, 1x3	060D9	174-3723-00
-24	131-1247-00		1	TERM,QIK DISC.:45 DEG BEND	00779	61664-1
-25	348-1619-00		2	GASKET, ELEC: CTS850	0KM03	9754219009
-26	441-2129-00		1	CHASSIS ASSY:ALUMINUM	TK1935	441212900
-27	426-2436-01		1	FRAME,CRT FLTR:POLYCARBONATE	TK1163	ORDER BY DESC
-28	348-1291-00		4	SHLD,GSK ELEK:CLIP-ON EM GASKET	30817	9760-5090-20
-29	640-0079-03		1	DISPLAY MONITOR:7 INCH,480X640 PIXEL	80009	640007903
-30	129-1450-01		1	SPACER,POST:0.640 OVERALL,0.25 HEX	80009	129-1450-01

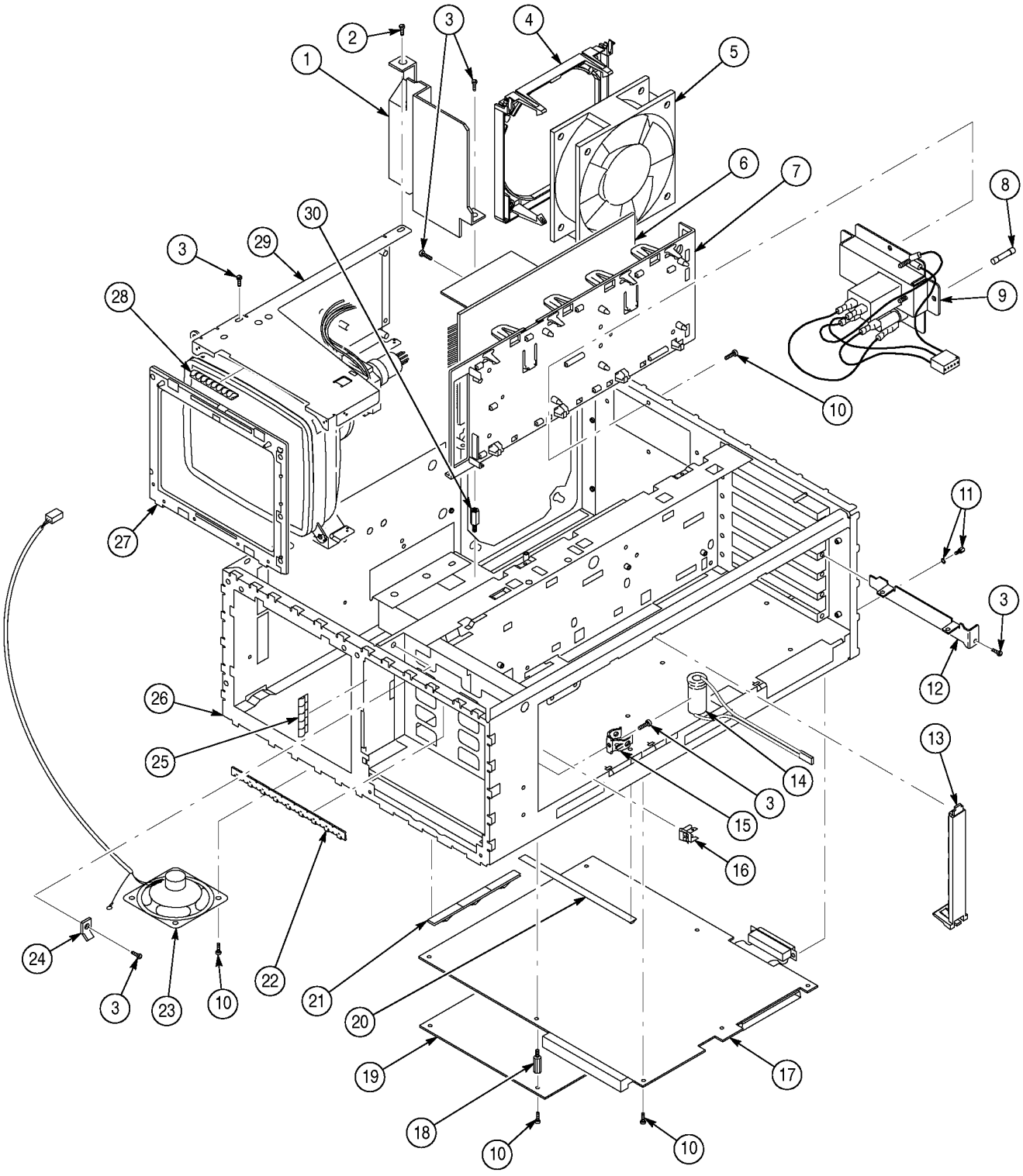


Figure 10-3: CRT and Mainframe

Fig. & Index No.	Tektronix Part No.	Serial No. Effective Dscont	Qty	12345	Name & Description	Mfr. Code	Mfr. Part No.
10-4							
-1	200-3660-00		1		COVER,AUTO CAL:POLYCARBONATE	TK1163	ORDER BY DESC
-2	337-4138-00		1		SHIELD,EMI:ALUM	80009	337413800
-3	213-0882-00				SCREW,TPG,TR:6-32 X 0.437,PNH,STL,CDPL,TYPETT	0KB01	ORDER BY DESC
-4	213-1079-00		6		JACKSCREW:4-40 X 0.250EXT THD	00779	745563-2
-5	671-3995-52		1		CIRCUIT BD ASSY: DISPLAY/CPU	80009	671399500
-6	672-1490-52		1		CIRCUIT BD ASSY:JAWA MAIN/DAUGH	80009	672149052
-7	672-1528-50		1		CIRCUIT BD ASSY:E(N)/DS3 TRIB MODULE	80009	672149152
-8	174-3792-00		1		CA ASSY, SP; RIBBON	53387	174379200
-9	174-3619-00		1		CA ASSY, RF; COAX; MMS	060D9	174361900
-10	174-3178-00		1		CA ASSY, SP; SHLD CMPST	53387	174317800
-11	174-3599-00		1		CA ASSY, RF; COAX; MMS	53387	174359900
-12	671-4546-00		1		CIRCUIT BD ASSY:CLOCK GENERATOR	80009	671454600
-13	671-4118-00		1		CIRCUIT BD ASSY:BACKPLANE	80009	671411800
-14	346-0133-00		1		STRAP,TIEDOWN,E:14.0 X 0.091,NYLON	59730	TY234M EURO DIR
-15	348-0150-00		1		GROMMET,PLASTIC:DK GRAY,U-SHAPE,0.66 ID	0KBZ5	348015000

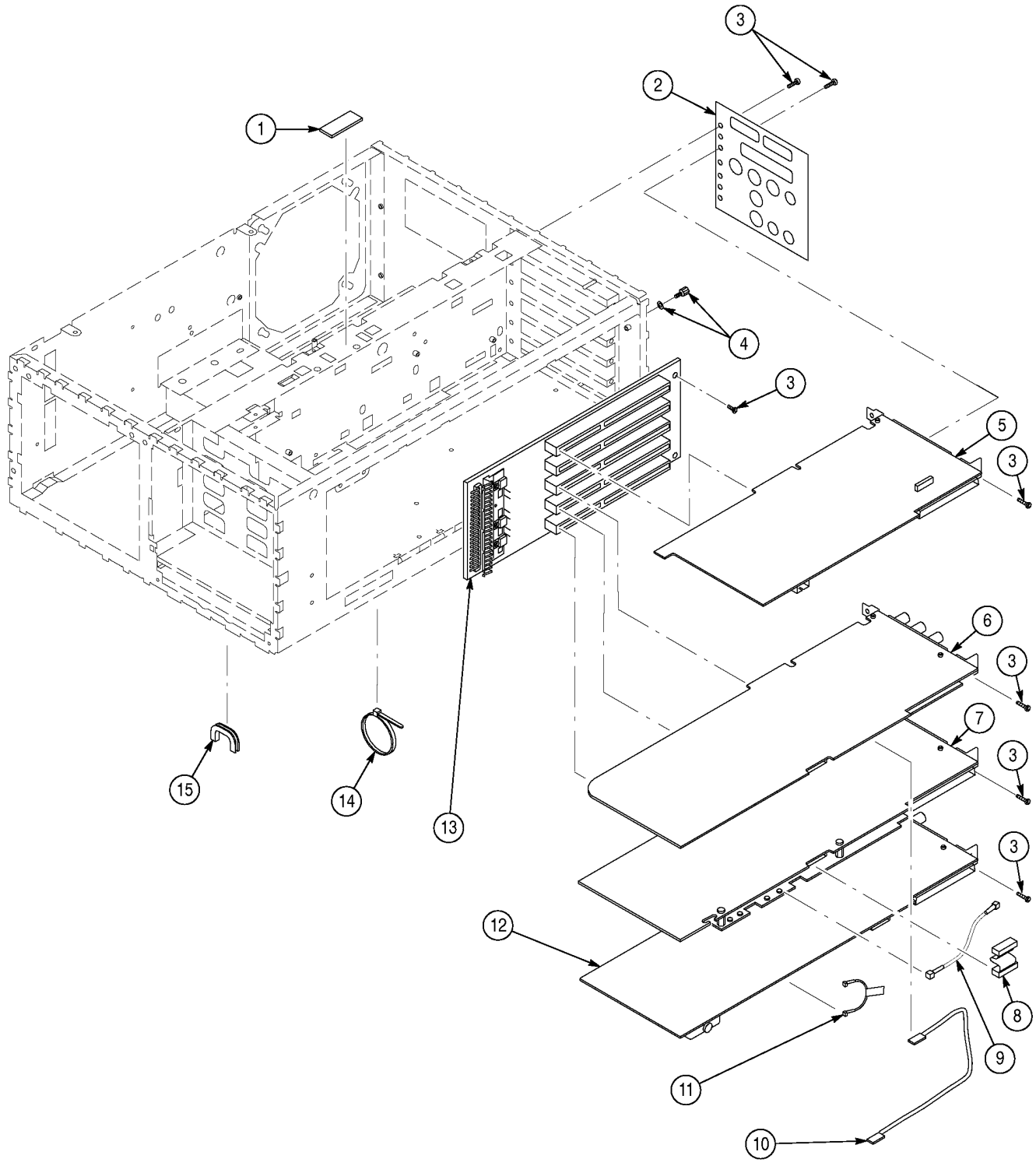


Figure 10-4: Circuit Boards

Fig. & Index No.	Tektronix Part No.	Serial No. Effective Dscont	Qty	12345	Name & Description	Mfr. Code	Mfr. Part No.
10-5							
-1	174-3044-01		1		CA ASSY,PWR:DESCRETE,;PSC,22,18 AWG,1X22	TK2469	174304400
-2	174-3938-00		1		CA ASSY,SP:	1DM20	174393800
-3	213-1061-00		1		JACKSCREW: 6-32 x 0.320 EXT THD	00779	554043-3
-4	174-3040-02		1		CA ASSY,SP:RIBBON,;HDI,100,30 AWG,0.025 CTR	53387	ORDER BY DESC
-5	174-3039-00		1		CA ASSY,SP:RIBBON,;HDI,100,30 AWG,0.025 CTR,9.0 L	53387	ORDER BY DESC
-6	174-3693-00		1		CA ASSY, SP: RIBBON, GPIB: IDC, 28 AWG, 18.0 L	060D9	174369300
-7	174-3038-00		1		CA ASSY,SP:RIBBON,;IDC/MLD,10,28 AWG,0.05 CTR,1.75 L	53387	174303800
-8	174-3699-00		1		CA ASSY,SP:FLAT FLEX,FLEX,27 AWG,6.0 L	TK2469	174369900
-9	174-3705-00		1		CA ASSY,SP:FLAT	TK2469	174228300
-10	174-2964-01		1		CA ASSY SP:FLAT FLEX,26,COND,300 V,1.5A,8.0 L	1DM20	174296401

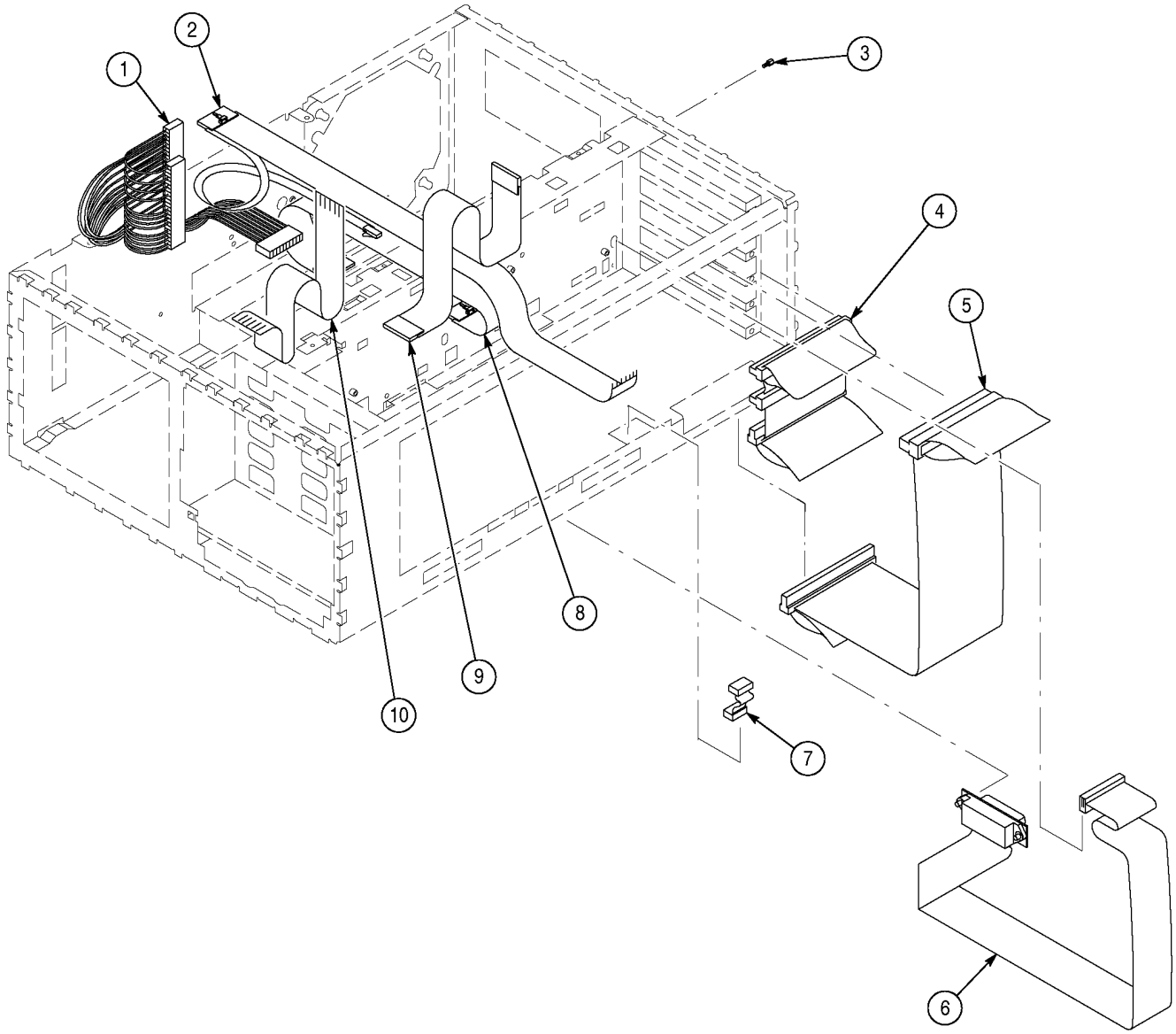


Figure 10-5: Cables

Fig. & Index No.	Tektronix Part No.	Serial No. Effective Dscont	Qty	12345	Name & Description	Mfr. Code	Mfr. Part No.
10-6					**STANDARD ACCESSORIES**		
-1	161-0066-00		1		CABLE ASSY,PWR (STANDARD)	80009	161006600
-2	161-0104-05		1		CA ASSY,PWR:3,1.0MM SQ,250V/10A,2.5 METER,RTANG (OPTION A3-AUSTRALIAN)	S3109	ORDER BY DESC
-3	161-0104-06		1		CA ASSY,PWR:3,1.0MM SQ,250V/10A,2.5 METER,RTANG (OPTION A1-EUROPEAN)	S3109	ORDER BY DESC
-4	161-0104-07		1		CA ASSY,PWR:3,1.0MM SQ,240V/10A,2.5 METER,RTANG (OPTION A2-UNITED KINGDOM)	S3109	ORDER BY DESC
-5	161-0104-08		1		CA ASSY,PWR:3,18 AWG,250/10A,98 INCH L,RTANG (OPTION A4-NORTH AMERICAN)	2W733	ORDER BY DESC
-6	161-0167-00		1		CA ASSY,PWR:3,0.75MM SQ,250V/10A,2.5 METER,RTANG (OPTION A5-SWITZERLAND)	S3109	ORDER BY DESC
	343-0170-00		1		RTNR,CA TO CA:U/W 0.25 OD CABLES (OPTIONS A1,A2,A3,A4,A5)	0JR05	ORDER BY DESC
	200-2265-00		1		CAP,FUSEHOLDER:5 X 20MM FUSES (OPTIONS A1,A2,A3,A4,A5)	61935	FEK 031.1663
	070-9988-01		1		MANUAL,REF:USER, ENGLISH, DP		070998800
	070-9990-01		1		MANUAL,REF:PROGRAMMER,ENGLISH,DP		070999000
					OPTIONAL ACCESSORIES		
	012-1469-00		1		CABLE,SIEMENS:CMPST,DIN41628;SDI ,3,120 OHM,BAL	TK2469	012146900
	012-1470-00		1		CABLE,INTCON:COAX,PATCH CORD;SDI,75 OHM,6.0L	70674	CC1756
	012-1471-00		1		CABLE,INTCON:COAX,;SDI,75 OHM,6.0 L,BNC,MALE	70674	CC1656
	016-1157-00		1		CASE,CARRYING:26 X 22 X 12,HARD TRANS W/WHEELS	34416	ORDER BY DESC
	016-1158-01		1		CASE,CARRYING:SOFT PADDED,OPTIONS	80009	016115800
	070-9991-00		1		MANUAL,TECH:SERVICE, ENGLISH		070999100
	070-9998-01		1		MANUAL,REF:USER,PORTUGUESE		070999800
	070-9996-01		1		MANUAL,REF:USER,ITALIAN		070999600
	071-0000-01		1		MANUAL,REF:USER,SPANISH		071000000

103-0365-00	1	ADAPTER,CONN RF:DSI BANTAM-WECO310 ADAPTER	70674	AP051
103-0366-00	1	ADAPTER,CONN:BNC-WECO 440,;BNC	14949	ADMW12
103-0367-00	1	ADAPTER,CONN:BNC-WECO 358;BNC,JACK,75 OHM	14949	AD1W
012-1338-00	1	CA ASSY, RF: COAX		
012-1364-00	1	CABLE, INTCON: CMPST, RJ45		
020-2317-00	1	WANDER ANALYST		
020-2318-00	1	USER MANUAL AND WANDER ANALYST		

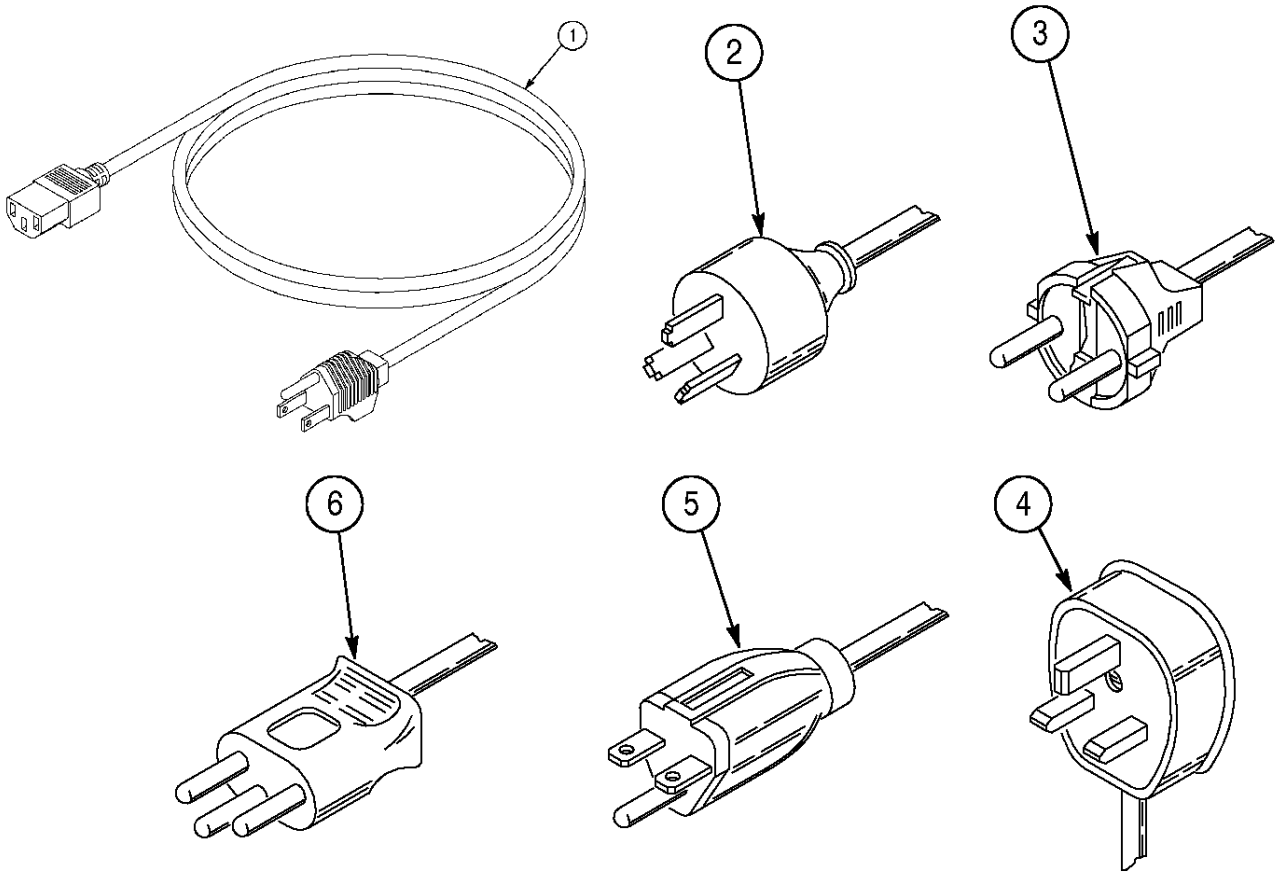


Figure 10-6: Power Cords

Glossary

ADM

An acronym for Add/Drop Multiplexer. A multiplexer capable of extracting and inserting lower-rate signals from a higher-rate multiplexed signal without completely demultiplexing the signal.

AIS

An acronym for Alarm Indication Signal. An AIS is used to alert downstream equipment that an upstream failure has been detected. In SONET, four categories of AIS are defined: Line AIS, STS Path AIS, VT Path AIS, Dsn AIS.

AMI

An acronym for Alternate Mark Inversion. The line-coding format in transmission systems where successive ones (marks) are alternatively inverted (sent with polarity opposite that of the preceding mark).

ANSI

An acronym for the American National Standards Institute. A standard-setting, non-government organization, which develops and publishes standards for “voluntary” use in the United States. It also coordinates U.S. participation in the International Standards Organization (ISO).

APS

An acronym for Automatic Protection Switching. Automatic Protection Switching is the ability of a network element to detect a failed working line and switch the service to a spare (protection) line. 1+1 APS pairs a protection line with each working line. 1:N APS provides one protection line for every N working lines.

ASCII

An acronym for American Standard Code for Information Interchange.

Asynchronous

A network where transmission system payloads are not synchronised and each network terminal runs on its own clock.

ATM

An acronym for Asynchronous Transfer Mode. A multiplexing/ switching technique in which information is organized into fixed-length cells with each cell consisting of an identification header field and an information field. The transfer mode is asynchronous in the sense that the use of the cells depends on the required or instantaneous bit rate.

Attenuation

Reduction of signal magnitude or signal loss, usually expressed in decibels.

AU

An acronym for Administrative Unit. An Administrative Unit is the information structure which provides adaptation between the Higher Order path layer and the multiplex section layer. The Administrative Unit consists of the Virtual Container (VC) plus the pointers (H1, H2, and H3 bytes).

Backhauling

Cumbersome traffic management technique used to reduce expense of multiplexing/demultiplexing.

Bandwidth

Information-carrying capacity of a communication channel. Analog bandwidth is the range of signal frequencies that can be transmitted by a communication channel or network.

BER

An acronym for Bit Error Ratio (or Rate). The principal measure of quality of a digital transmittion system. BER is defined as:

$$BER = \frac{Number\ of\ Errors}{Total\ Number\ of\ Bits}$$

BER is usually expressed as a negative exponent. For example, a BER of 10^{-7} means that 1 bit out of 10^{7} bits is in error.

Bidirectional

Operating in both directions. Bidirectional APS allows protection switching to be initiated by either end of the line.

BIP
An acronym for Bit Interleaved Parity. A method used to monitor errors in the transmitted signal.

BISDN
An acronym for Broadband Integrated Services Digital Network. It defines a single ISDN network which can handle voice, data, and eventually video services.

Bit
One binary digit; a pulse of data.

Bit Error
An incorrect bit. Also known as a coding violation.

Bit Synchronous
A way of mapping payload into virtual tributaries that synchronizes all inputs into the Vts, but does not capture any framing information or allow access to subrate channels carried in each input. For example, bit synchronous mapping of a channeled DS1 into a VT1.5 does not provide access to the DS0 channels carried by the DS1.

Bit stuffing
In asynchronous systems, a technique used to synchronise asynchronous signals to a common rate before multiplexing.

Bits per second (bit/s or bps)
The number of bits passing a point every second. The transmission rate for digital information.

Broadband
Services requiring over 2 Mbit/s transport capacity.

Byte-interleaved
Bytes from each STS-1 are placed in sequence in a multiplexed or concatenated STS-N signal. For example, for an STS-3, the sequence of bytes from contributing STS-1s is 1, 2, 3, 1, 2, 3. . .

Byte synchronous

A way of mapping payload into virtual tributaries that synchronizes all inputs into the Vts, captures framing information, and allows access to subrate channels carried in each input. For example, byte synchronous mapping of a channeled DS1 into a VT1.5 provides direct access to the DS0 channels carried by the DS1.

CCITT

The technical organs of the United Nations specialized agency for telecommunications, now called the International Telecommunications Union (ITU). They function through international committees of telephone administrations and private operating agencies.

Channel

The smallest subdivision of a circuit that provides a type of communication service; usually a path with only one direction.

Circuit

A communications path or netwrok; usually a pair of channels providing bidirectional communication.

Circuit Switching

Basic switching process whereby a circuit between two users is opened on demand and maintained for their exclusive use for the duration of the transmission.

Coding Violation (CV)

A coding violation is an error detected by Bit-Interleaved Parity (BIP) checks.

COFA

An acronym for Change of Frame Alignment.

Concatenation

The linking together of various data structures. For example, two channels joined to form a single channel. In SDH, a number (M) of Tus can be linked together to produce a concatenated container, M times the size of the TU. An example of this is the concatenation of five TU-2s to carry a 32 Mbit/s video signal, known as VC-2-5c. Once assembled, any concatenated VC structure is multiplexed, switched and transported through the network as a single entity.

Concatenated STS-Nc
A signal in which the STS Envelope Capacities from the N STS-1s have been combined to carry an STS-Nc Synchronous Payload Envelope (SPE). It is used to transport signals that do not fit into an STS-1 (52 Mb/s) payload.

CRC
An acronym for Cyclic Redundancy Check. The CRC is a technique for using overhead bits to detect transmission errors.

dB
The symbol for Decibels.

dBm
The symbol for power level in decibels relative to 1mW.

DCC
An acronym for Data Communications Channel. These are data channels in SONET/SDH that enable OAM&P communications between intelligent controllers and individual network nodes as well as internode communications.

Defect
A limited interruption in the ability of an item to perform a required function. Persistence of a defect can cause a failure.

DCS
An acronym for Digital Cross-connect. A DCS is an electronic cross-connect which has access to lower-rate channels in higher-rate multiplexed signals and can electronically rearrange (cross-connect) those channels.

Digital Signal
An electrical or optical signal that varies in discrete steps. Electrical signals are coded as voltages, optical signals are coded as pulses of light.

DSX-1
May refer to either a cross-connect for DS1 rate signals or the signals cross-connected at a DSX-1.

DSX-3
May refer to either a cross-connect for DS3 rate signals or the signals cross-connected at a DSX-1.

ECSA

An acronym for Exchange Carrier Standards Association. ECSA is an organization that specifies telecommunications standards for ANSI.

EIA

An acronym for Electronics Industry Association.

Envelope capacity

The number of bytes the payload envelope of a single frame can carry. The SONET STS payload envelope is the 783 bytes of the STS-1 frame available to carry a signal. Each virtual tributary has an envelope capacity defined as the number of bytes in the virtual tributary less the bytes used by VT overhead.

ETSI

An acronym for the European Telecommunications Standards Institute). ETSI is an organization responsible for defining and maintaining European standards, including SDH.

Failure

A termination of the ability of an item to perform a required function. A failure is caused by the persistence of a defect. A failure is a defect that persists beyond the maximum time allocated to the transmission system protection mechanisms.

FEBE

An acronym for Far End Block Error. An indication returned to the transmitting LTE that an errored block has been detected at the receiving LTE. *(FEBE is currently called REI).*

FERF

An acronym for Far End Receive Failure. A FERF indicates to the transmitting LTE that the receiving LTE has detected an incoming line failure or is receiving a Line AIS. *(FERF is currently called RDI).*

Fixed Stuff

A bit or byte whose function is reserved. Fixed stuff locations, sometimes called reserved locations, do not carry overhead or payload.

Floating Mode
A virtual tributary mode that allows the VT/VC synchronous payload envelope to begin anywhere in the VT/VC. Pointers identify the starting location of the VT SPE/LO-VC. VT SPEs/LO-VCs in different superframes/multiframes may begin at different locations.

Framing
Method of distinguishing digital channels that have been multiplexed together.

Frequency
The number of cycles of periodic activity that occur in a discrete amount of time.

Grooming
Consolidating or segregating traffic for efficiency.

Interleave
The ability of SONET/SDH to mix together and transport different types of input signals in an efficient manner, thus allowing higher transmission rates.

Isochronous
All devices in the network derive their timing signal directly or indirectly from the same primary reference clock.

ITU
An acronym for International Telecommunication Union (formerly CCITT). ITU is an agency of the United Nations responsible for the regulation, standardization, coordination, and development of international telecommunications as well as the harmonization of national policies. It functions through international committees of telecommunications administrations, operators, manufacturers, and scientific/industrial organizations.

Jitter
The short term variations of the significant instants of a timing signal from their ideal positions in time (where short term implies that these variations are of frequency greater than or equal to 10 Hz). Short waveform variations caused by vibration, voltage fluctuations, control system instability, etc.

Line

The portion of a transmission line between two multiplexers. One or more SONET sections, including network elements at each end, capable of accessing, generating, and processing Line Overhead.

Line AIS (Alarm Indication Signal)

A Line AIS is generated by Section Terminating Equipment upon the detection of a Loss of Signal or Loss of Frame defect, or an equipment failure. AIS-L maintains operation of the downstream regenerators, therefore preventing generation of unnecessary alarms. At the same time, data and orderwire communication is retained between the regenerators and the downstream Line Terminating Equipment (LTE).

Line Coding Violations (CVs)

Line Cvs are the sum of the BIP errors detected at the Line layer. Line Cvs are collected using the BIP codes in the B2 bytes of the Line overhead.

Line FERF

See Line RDI.

Line RDI (Remote Defect Indication)

A signal returned to the transmitting LTE upon detecting a Loss of Signal, Loss of Frame, or AIS-L defect. *(RDI-L was previously known as Line FERF).*

Locked Mode

A virtual tributary mode that fixes the starting location of the VT SPE/VC. Locked mode has less pointer processing than floating mode.

LOF

An acronym for Loss of Frame.

LOH

An acronym for Line Overhead. LOH is 18 bytes of overhead accessed, generated, and processed by Line Terminating Equipment (LTE). This overhead supports functions such as locating the SPE in the frame, multiplexing or concatenating signals, performance monitoring, automatic protection switching and line maintenance.

LOP
An acronym for Loss of Pointer.

LOS
An acronym for Loss of Signal.

LTE
An acronym for Line Terminating Equipment.

Mb/s
An abbreviation for megabits per second.

mapping
The process of placing a tributary signal into a SONET SPE or a SDH AU.

Mesochronous
A network whereby all nodes are timed to a single clock source, thus all timing is exactly the same (truly synchronous).

MS-AIS
An acronym for Multiplex Section Alarm Indication Signal. MS-AIS is generated by Section Terminating Equipment upon the detection of a Loss of Signal or Loss of Frame defect, on an equipment failure. MS-AIS maintains operation of the downstreams regenerators, and therefore prevents generation of unnecessary alarms. At the same time, data and orderwire communication is retained with the downstream Line Terminating Equipment.

MS-RDI
An acronym for Multiplex Section Remote Defect Indication. MS-RDI is a signal returned to the transmitting Line Terminating Equipment upon detecting a Loss of Signal, Loss of Frame, or MS-AIS defect. MS-RDI was previously known as Multiplex Section FERF.

MSOH
An acronym for Multiplex Section Overhead. MSOH is eighteen bytes of overhead accessed, generated, and processed by MS terminating equipment. This overhead supports functions such as locating the payload in the frame, multiplexing or concatenating signals, performance monitoring, automatic protection switching, and line maintenance.

Multiframe
Any structure made of multiple frames. SDH has facilities to recognize multiframes at the E1 level and at the VC-n level.

Multiplexer
A device for combining several channels to be carried by one line or fiber.

Narrowband
Services requiring up to 1.5 Mbit/s transport capacity.

NE
An acronym for Network Element. In SDH, the five basic network elements are:

- ◊ add/drop multiplexer
- ◊ broadband digital cross-connect
- ◊ wideband digital cross-connect
- ◊ flexible multiplexer
- ◊ regenerator

Any device which is part of an SDH transmission path and serves one or more of the section, line, and path-terminating functions.

In SONET, the five basic network elements are:

- ◊ add/drop multiplexer
- ◊ broadband digital cross-connect
- ◊ wideband digital cross-connect
- ◊ digital loop carrier
- ◊ switch interface

Any device which is part of a SONET transmission path and serves one or more of the section, line, and path-terminating functions.

OAM
An acronym for Operations, Administration, and Maintenance.

OAM&P
An acronym for Operations, Administration, Maintenance, and Provisioning. It provides the facilities and personnel required to manage a network.

OC
An acronym for Optical Carrier.

OC-N (Optical Carrier Level N)
An optical version of an STS-N signal.

OOF
An acronym for Out of Frame.

Orderwire
A dedicated voice channel used by installers to expedite the provisioning of lines.

OS
An acronym for Operations System. OS is a sophisticated applications software that manages operation of the entire network.

OSI Seven-Layer Model
A standard architecture for data communications. Layers define hardware and software required for multi-vendor information processing equipment to be mutually compatible. The seven layers from lowest to highest are: physical, link, network, transport, session, presentation, and application.

Overhead
Extra bits in a digital stream used to carry information besides traffic signals. Orderwire, for example, would be considered overhead information.

Packet Switching
An efficient method for breaking down and handling high-volume traffic in a network. A transmission technique that segments and routes information into discrete units. Packet switching allows for effieicne tsharing of network resources as packets from different sources can all be sent over the same channel in the same bitstream.

Parity check
An error-checking scheme which examines the number of transmitted bits in a block which hold the value of “one”. For even parity, an overhead parity bit is set to either one or zero to make the total number of transmitted ones in the data block plus parity bit an even number. For odd parity, the parity bit is set to make the total number of ones in the block an odd number.

Path
The portion of a SONET/SDH transmission network between two terminal multiplexers.

Path Overhead
A set of bytes allocated within the information payload (SPEVC) to carry status and maintenance information between terminal equipment along the same path as the information; overhead accessed, generated, and processed by path-terminating equipment. Path Overhead includes nine bytes of STS Path Overhead, and when the frame is VT-structured, five bytes of VT Path Overhead.

Payload
The portion of the SONET/SDH signal available to carry service signals such as DS1, DS2, DS3, E1 and E3. The contents of a STS SPE, VT SPE, or VC.

Payload Pointer
Indicates the beginning of a Synchronous Payload Envelope or Virtual Container.

Payload capacity
The number of bytes the payload of a single frame can carry.

Photonic
The basic unit of light transmission used to define the lowest (physical) layer in the OSI seven-layer model.

Plesiochronous
A network with nodes timed by separate clock sources with almost the same timing.

POH
An acronym for Path Overhead.

Pointer
A part of the SONET/SDH overhead that locates a floating payload structure. STS/U-n pointers locate the payload. VT/TU-m pointers locate floating mode virtual tributaries. All SONET/SDH frames use STS/AU pointers; only floating mode virtual tributaries/containers use VT/TU pointers.

Poll

An individual control message from a central controller to an individual station on a multipoint network inviting that station to send.

POP

An acronym for Point of Presence. POP is a point in the network where inter-exchange carrier facilities like DS3 or OC-n meet with access facilities managed by telephone companies or other service providers.

PRC

An acronym for Primary Reference Clock. In a synchronous network, all the clocks are traceable to one highly stable reference supply, the PRC. The accuracy of the pRC is better than ± 1 in 10^{11} and is derived from a cesium atomic standard.

PTE

An acronym for Path Terminating Equipment. PTE are network elements such as fiber optic terminating systems which can access, generate, and process Path Overhead.

RAI

An acronym for Remote Alarm Indication. RAI is a code sent upstream in a DSn/E-n network as a notification that a failure condition has been declared downstream. *(RAI signals were formerly known as Yellow signals).*

RDI

An acronym for Remote Defect Indication. RDI is a signal returned to the transmitting Terminating Equipment when the receiving Terminating Equipment detects a Loss of Signal, Loss of Frame, or AIS defect. *(RDI was formerly known as FERF).*

REI

An acronym for Remote Error Indication. REI is an indication returned to a transmitting node (source) that an errored block has been detected at the receiving node (sink). *(REI was formerly known as FEBE).*

RFI

An acronym for Remote Failure Indication. When a defect has become a failure, an RFI is sent to the far end and will initiate a protection switch if this function has been enabled.

Regenerator
Device that restores a degraded digital signal for continued transmission; also called a repeater.

Rx
An abbreviation for Receiver.

SDH
An acrnym for Synchronous Digital Hierarchy. SDH is the ITU-defined international networking standard whose base transmission level is 155 Mbit/s (STM-1). SDH standards were first published in 1989 to address interworking between the ITU and ANSI transmission hierarchies.

SEC
An acronym for Synchronous Equipment Clock. SEC is a standard slave clock contained within an SDH network element as defined by the g.813 ITU standard.

Section
The portion of a transmission line between a Network Element (NE) and a Multiplex Section or Line Terminating Equipment (TE) or two Multiplex Section or Line TEs.

Section Coding Violations (CVs)
Section Cvs are BIP errors that are detected at the Section layer. CVs for the Section layer are collected using the BIP-8 in the B1 byte located in the Section overhead of STS-1 number 1.

Slip
An overflow (deletion) or underflow (repetition) of one frame of a signal in a receiving buffer.

SOH
An acronym for Section Overhead. SOH is a set of bytes allocated within each frame to carry framing and error monitoring information between repeaters along the same path as the information. Section Overhead contains nine bytes of overhead accessed, generated, and processed by section terminating equipment. This overhead supports functions such as framing the signal and performance monitoring.

SONET

An acronym for Synchronous Optical NETwork. A standard for optical transport that defines optical carrier levels and their electrically equivalent synchronous transport signals. SONET allows for a multi-vendor environment and positions the network for transport of new services, synchronous networking, and enhanced OAM&P.

SPE

An acronym for Synchronous Payload Envelope. The major portion of the SONET frame format used to transport payload and STS path overhead. A SONET structure that carries the payload (service) in a SONET frame or virtual tributary. The STS SPE may begin anywhere in the frame's payload envelope. The VT SPE may begin anywhere in a floating mode VT, but begins at a fixed location in a locked-mode VT.

SSU

An acronym for Synchronisation Supply Unit. An SSU is a network equipment clock.

STE

An acronym for Section Terminating Equipment. STE interprets and modifies or creates the Section Overhead.

STM

An acronym for Synchronous Transport Module. STM is a structure in the SDH transmission hierarchy. STM-1 is the basic SDH building block signal transmitted at 155.52 Mb/s data rate.

STM-N

An acronym for Synchronous Transport Module-N (STM-1, -4, -16). The different STM-N rates are listed in the following table. The table below also includes the ANSI designation for the equivalent SONET rates.

SDH/SONET Signal Hierarchy

SDH Designation	Data Rate (Mb/s)	SONET Designation	
		Electrical Signal	Optical Signal
	51.48	STS-1	OC-1
STM-1	155.52	STS-3	OC-3
STM-4	622.08	STS-12	OC-12
STM-16	2488.32	STS-48	OC-48

STS

An acronym for Synchronous Transport Signal. STS is a structure in the SONET transmission hierarchy. STS-1 is the basic SONET building block signal transmitted at 51.84 Mb/s data rate.

STS-N

An acronym for Synchronous Transport Signal level-N (STS-1,-3,-12,-48). The signal obtained by multiplexing integer multiples (N) of STS-1 signals together. The different STS-N rates (and their optical equivalents) are listed in the following table. The table below also includes the ITU-T Synchronous Digital Hierarchy (SDH) designation for the equivalent SDH rates.

SONET/SDH Signal Hierarchy

SONET Designation			
Electrical Signal	**Optical Signal**	**Data Rate (Mb/s)**	**SDH Designation**
STS-1	OC-1	51.48	
STS-3	OC-3	155.52	STM-1
STS-12	OC-12	622.08	STM-4
STS-48	OC-48	2488.32	STM-16

STS POH

An acronym for STS Path Overhead. Nine evenly distributed Path Overhead bytes per 125 micoseconds starting at the first byte of the STS SPE. STS POH provides for communication between the point of creation of an STS SPE and its point of disassembly.

STS RDI

An acronym for STS Path Remote Defect Indication. A signal returned to transmitting STS PTE upon setection of certain defects on the incoming path.

STS PTE

An acronym for STS Path Terminating Equipment. Equipment that terminates the SONET STS Path layer. STS PTE interprets and modifies or creates the STS Path Overhead. An NE that contains STS PTE will also contain LTE and STE.

Superframe
Any structure made of multiple frames. SONET recognizes superframes at the DS1 level (D4 and extended superframe) and at the VT (500u STS superframes).

Synchronous
A network where transmission system payloads are synchronised to a master (network) clock and traced to a reference clock. A network where all clocks have the same long term accuracy under normal operating conditions.

T1X1 Subcommittee
A committee within the ECSA that specifies SONET optical interface rates and formats.

Tributary
The lower rate signal input to a multiplexer for combination (multiplexing) with other low rate signals to form a higher rate signal.

TU
An acronym for Tributary Unit (SDH). A Tributary Unit is an information structure which provides adaption between the Lower-Order path layer and the Higher-Order path layer. It contains the Virtual Container plus a tributary unit pointer.

TUG
An acronym for Tributary Unit Group (TUG).

TE
An acronym for Terminal Equipment.

Through Mode
The ability to retransmit the incoming signal without changing its contents.

Transport Overhead
A set of bytes allocated within each frame to carry status and maintenance information between terminal equipment along the same path as the information.

TOH
An acronym for Transport Overhead.

Tx
An abbreviation for Transmitter.

VC
An acronym for Virtual Container. VC is a signal designed for transport and switching of sub-SDH payloads.

VT
An acronym for Virtual Tributary. A VT is a signal designed for transport and switching of sub-STS-1 payloads.

Wander
The long term variations of the significant instants of a digital signal from their ideal position in time (where long term implies that these variations are of frequency less than 10 Hz).

Wideband
Services requiring 1.5-50 Mb/s transport capacity.

Yellow Signal
An indication returned to a transmitting node (source) that an errored block has been detected at the receiving node (sink). *(Yellow signal is currently referred to as RAI).*